UNIT – VI

DIGITAL METERS

Digital Voltmeters:

The digital voltmeters are generally referred as DVM, convert the analog signals into digital and display the voltages to be measured as discrete numerical instead of pointer deflection, on the digital displays. Such voltmeters can be used to measure ac and dc voltages and also to measure the quantities like pressure, temperature, and stress etc, Using proper transducer and signal controlling circuit. The transducer converts the quantity into proportional voltage signal and signal conditioning circuit brings the signal into the proper limits which can be easily measured by the digital voltmeter. The output voltage is displayed on the digital display on the front panel. Such a digital output reduces the human reading and interpolation errors and parallax errors.

The DVM have various features and the advantages, over the conventional analog voltmeters having pointer deflection on the continuous scale.

Advantages of Digital Voltmeters:

The DVMs have number of advantages over conventional analog voltmeters, which are,

1. Due to the digital display, the human reading errors, interpolation errors and parallax errors are reduced.
2. They have input range from +1.000 V to +1000 V with the automatic range selection and the overload indication.
3. The accuracy is high up to ± 0.005% of the reading.

4. The resolution is better as 1μV reading can be measured on 1 V range.
5. The input impedance is as high as 10MΩ.
6. The reading speed is very high due to digital display.
7. They can be programmed and well suited for computerized control.
8. The output in digital form can be directly recorded and it is suitable for further processing also.

Comparison of Analog and Digital Instruments:

Sl.no	Parameter	Analog	Digital
1.	Accuracy	Less up to ± 0.1% of full scale	Very high accuracy up to ± 0.005% of reading.
2.	Resolution	Limited up to 1 part in several hundreds	high upto 1 part in several thousands
3.	Power	Power required is high hence can cause loading	Negligible power is required hence no loading effects
4.	cost	Low in cost	High cost compared to analog but now-a-days cost of digital instruments is also going down
5.	Frictional errors	Errors due to moving parts are present	no moving parts hence no errors
6.	Range & Polarity	No facility of auto ranging and auto polarity	Has the facility of auto ranging and auto polarity
7.	Input impedance	Low input impedance	Very high input impedance
8.	Observational errors	Errors such as parallax errors and approximation errors are present	Due to digital displays, the observational errors are absent.

9.	Compatibility	not compactable with modern digital instruments	The digital output can be directly fed into memory of modern digital instruments
10.	Speed	Reading speed is low	Reading speed is very high
11.	Programming facility	Not available	Can be programmed and well suited for the computerized control

Basic Block Diagram of DVM:

Any digital instrument requires analog to digital converter at its input. Hence first block in a general DVM is ADC as shown in fig.1

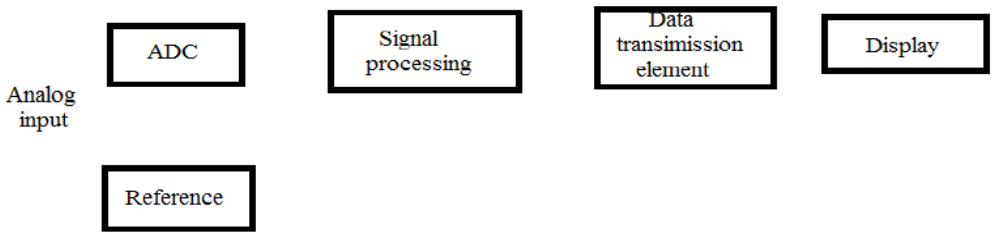


Fig.1 Basic block diagram of DVM

Every ADC requires a reference. The reference **is** generated internally and reference generator circuitry depends on the type of ADC technique used. The output of ADC is decoded and signal is processed in the decoding stage. Such a decoding is necessary to drive the seven segment display. The data from decoder is then transmitted to the display. The data transmission element may be a latches, counters etc, as per the requirement. A digital display shows the necessary digital result of the measurement.

Classification of Digital Voltmeters:

The digital voltmeters are classified mainly based on the technique used for the analog to digital conversion. Depending on this the digital voltmeters are mainly classified as,

1. Non-integrating type
    a) successive approximation type
    b) linear ramp type
2. Integrating type
    a) Dual slope integrating type

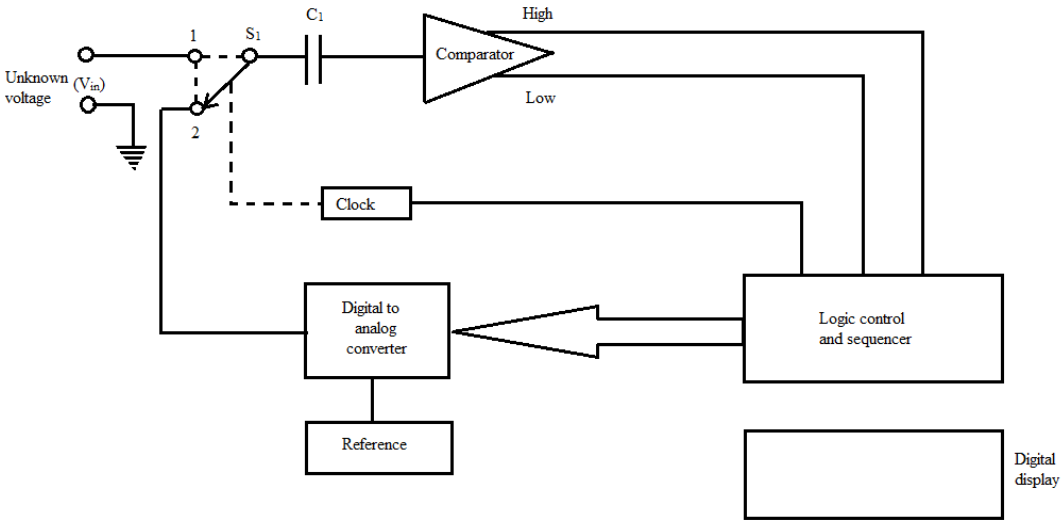
Successive Approximation Type DVM

The potentiometer used in the servo balancing type DVM is a linear but in successive approximation type a digital divider is used.. the digital divider is nothing but a digital to analog (D/A) converter. The servo motor is replaced by an electronic logic.

The basic principle of measurement by this method is similar to the simple example of determination of weight of the object. The object is placed on one side of the balance and the approximate weight is placed on the other side. If weight is more, the weight is removed and smaller weight is placed. If this weight is smaller then the object, another small weight is added, to the weight present. If now the total weight is higher than the object, the added weight is removed and smaller weight is added. Thus by such successive procedure if adding and removing, the weight of the object is determined. The successive approximation type DVM works exactly on the same principle.

In successive approximation type DVM, the comparator compares the output of digital to analog converter with the unknown voltage. Accordingly, the comparator provides logic high or low signals. The digital to analog converter successively generates the set pattern of signals. The procedure continues till the output of the digital to analog converter becomes equal to the unknown voltage.

The fig shows the block diagram of successive approximation type DVM.



The capacitor is connected at the input of the comparator. The output of the digital to analog converter is compared with the unknown voltage, by the comparator. The output of the comparator is given to the logic control and sequencer. This unit generates the sequence of code which is applied to digital to analog converter. The position 2 of the switch S_1 receives the output from digital to analog converter. The unknown voltage is available at the position 1 of the switch S_1. The logic control also drives the clock which is used to alternate the switch S_1 between the position 1 and 2, as per the requirement.

Consider the voltage to be measured is 3.7924 V. The set pattern of digital to analog converter is say 8-4-2-1. At the start, the converter generates 8v and switch is at the position 2. The capacitor C_1 charges to 8V. the clock is used to change the switch position. So during next time interval, switch position is 1 and unknown input is applied to the capacitor. As capacitor is charged to 8V which is more than the input voltage 3.7924 V, the comparator sends HIGH signal to the logic control and sequencer circuit. The HIGH signal resets the digital to analog converter which generates its next step of 4v. this again generates HIGH signal. This again resets the converter to generate the next step of 2 V.

Now 2V is less than the input voltage. The comparator generates LOW signal and sends it to logic control and sequence circuit. During the generation of LOW signal, the generated signal by the converter is retained. Thus the 2v step gets stored in the converter. In addition to this, next next step of 1Vis generated. Thus the total voltage level becomes, stored 2 + generated 1 i.e. 3V. this is again less than the input and generates LOW signal. Due to

low signal. This gets stored . after this 0.8V step is generated for the second digit approximation.

Thus the process of successive approximation continues till the converter generates 3.7924 V. This voltage is then displayed on the digital display.

At each low signal, there is an incremental change in the output of the digital toi analog converter. This output voltage approaches the value of the unknown voltage. The limit to how close this output can approach to the unknown voltage, depends on the level of noise at the input of the comparator and the stability of the input switch. To reduce the noise, filters may be used but it reduces the speed of measurement. These limiting factors usually determine the number of digits of resolution of an instrument. The general range of digits is 3 to 5. The speed depends upon the type of switches are used in digital to analog converter and comparator circuitry. If solid state switches are used, the high speed can be obtained. For electromechanical switches, the speed is few readings per second. The accuracy depends on the internal reference supply associated with the digital to analog converter and the accuracy of the converter itself.

Advantages:

The advantages of successive approximation DVM are,

1. Very high speed of the order of 100 readings per second possible.
2. The method of ADC is inexpensive.
3. The resolution upto 5 significant digits is possible.
4. The accuracy is high.

Disadvantages:

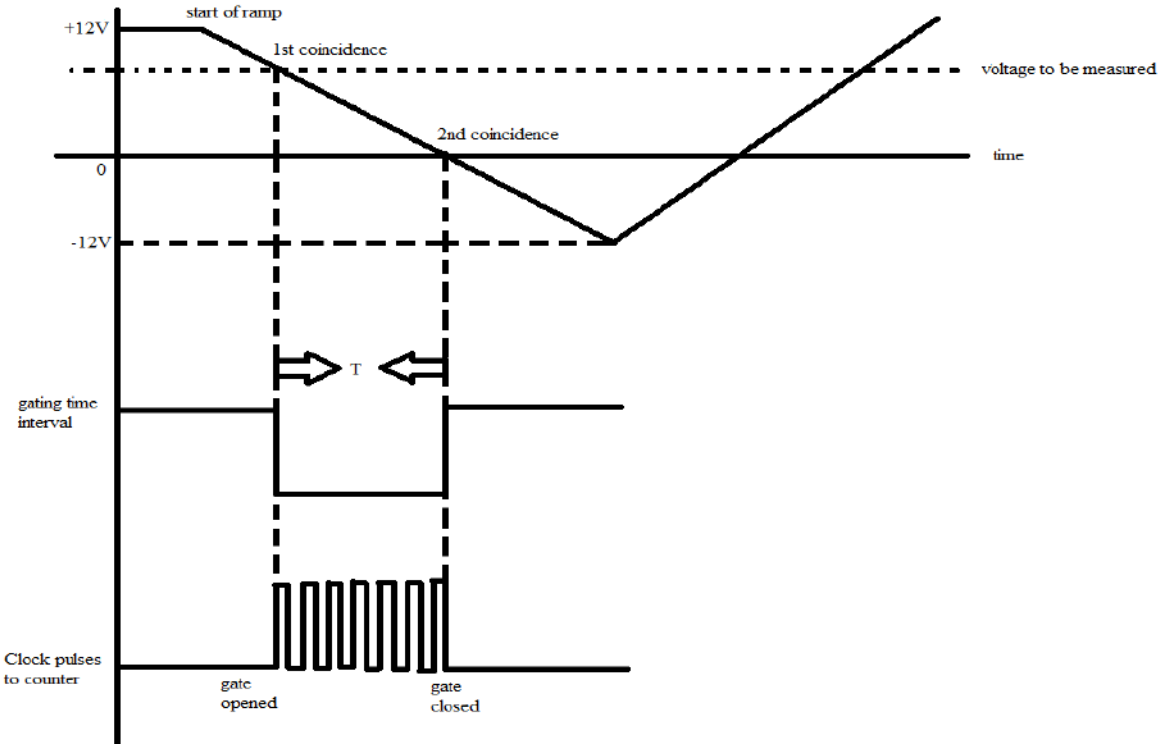
The disadvantages of successive approximation type DVM are,

1. The circuit is complex.
2. The DAC is also required.
3. The input impedance is variable.
4. The noise can cause error due to incorrect decisions made by comparator.

Linear Ramp Technique:

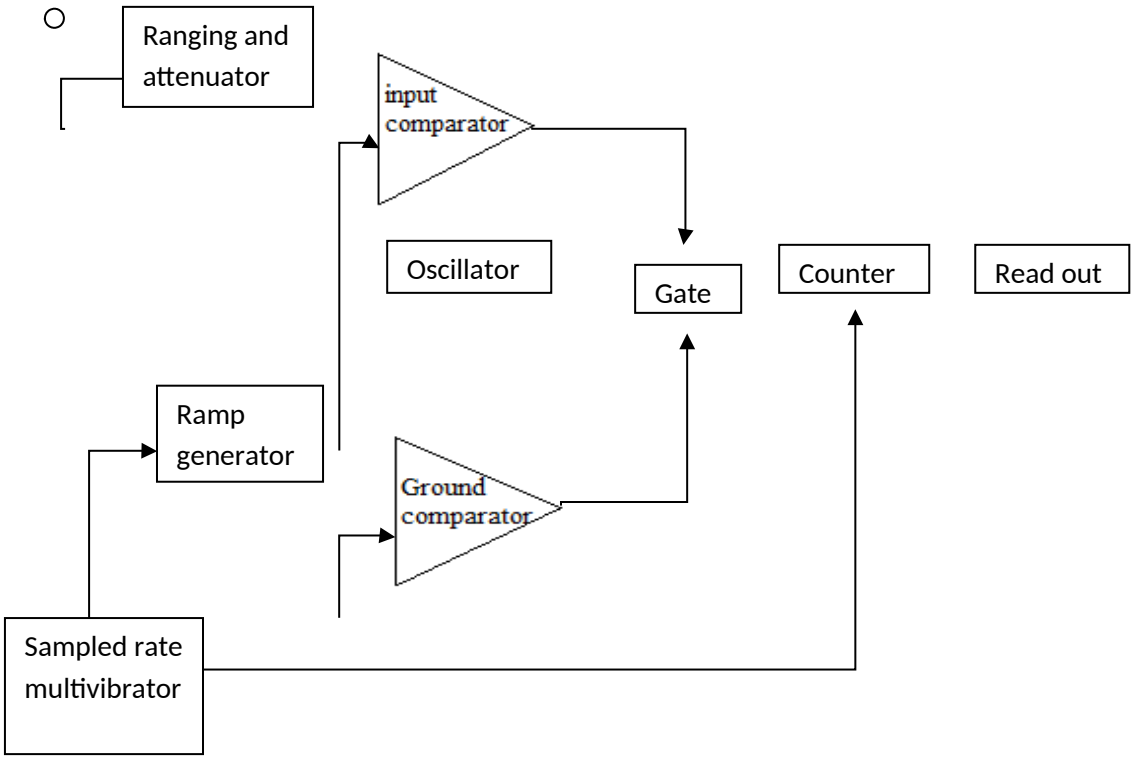
The basis principle of such measurement is based on the measurement of the time taken by a linear ramp to rise from 0V to the level of the input voltage or to decrease from the level of the input voltage to zero. This time is measured with the help of electronic time interval counter and the count is displayed in the numeric form with the help of a digital display.

Basically it consists of a linear ramp which is positive going or negative going. The range of the ramp is ± 12V while the base range is ± 10V. the conversion from a voltage to a time interval is shown in fig.9.10.1



At the start of measurement, a ramp voltage is initiated which is continuously compared with the input voltage. When these two voltages are same, the comparator generates a pulse which opens a gate i.e. the input comparator generates a start pulse. The ramp continues to decrease and finally reaches to 0V or ground potential. This is sensed by the second comparator or ground comparator. At exactly 0V, this comparator produces a stop pulse which closes the gate. The number of clock pulses are measured by the counter. Thus the time duration for which the gate is opened, is proportional to the input voltage. In the time interval between start and stop pulses, the gate remains open and the oscillator circuit drives the counter. The

magnitude of the count indicates the magnitude of the input voltages, which is displayed by the display. The block diagram of linear ramp DVM is shown in fig. 9.10.2.



Properly attenuated input signal is applied as one input to the input comparator. The ramp generator generates the proper linear ramp signal which is applied to the both the comparators. Initially the logic circuit sends a reset signal to the counter and the readout. The comparators are designed in such a way that when both the input signals of comparator are equal then only the comparator changes its state. The input comparator is used to send the start pulse while the ground comparator is used to send stop pulse.

When the input and ramp are applied to the input comparator and at the point when negative going ramp becomes equal to the input voltages the comparator sends start pulse, due to which gate opens. The oscillator drives the counter. The counter starts counting the pulses received from the oscillator. Now the same ramp is applied to the ground comparator becomes zero (grounded) i.e. equal and it sends a stop pulse to the gate due to which gate gets closed. Thus the counter stops receiving the pulses from the local oscillator. A definite number of pulses will be

counted by the counter, during the start and stop pulses which is measure of the input voltage. This is displayed by the digital readout.

The sample rate multivibrator determines the rate at which the measurement cycles are initiated. The oscillation of this multivibrator is usually adjusted by a front panel control named rate, from a few cycles per second to as high as 1000 or more cycles per ±0.005% of the reading. The sample rate provides an initiating pulse to the ramp generator to start its next ramp voltage. At the same time, a reset pulse is also generated which resets the counter to the zero state.

The advantages of this technique sre:

1. The circuit is easy to design
2. The cost is low.
3. The output pulse can be transferred over long feeder lines without loss of information.
4. The input signal is converted to time, which is easy to digitize.
5. By adding external logic, the polarity of the input also can be displayed.
6. The resolution of the readout is directly proportional to the frequency of the local oscillator. So adjusting the frequency of the local oscillator, better resolution can be obtained.

The disadvantages of this technique are:

1. The ramp requires excellent characteristics regarding its linearity.
2. The accuracy depends on the slope of the ramp and stability of the local oscillator.
3. Large errors are possible if noise is superimposed on the input signal.
4. The offsets and drifts in the two comparators may cause errors.
5. The speed of measurement is low.
6. The swing of the ramp is ±12V, this limits the base range of measurement to ±10V.

Dual Slope Integrating Type DVM:

This is the most popular method of analog to digital conversion. In the ramp techniques, the noise can cause large errors but in dual slope method the noise is averaged out by the positive and negative ramps using the process of integration. The basic principle of this method is that the input signal is integrated for a fixed interval of time. And then the same integrator is used

to integrate the reference voltage with reverse slope. Hence the name given to the technique is dual slope integration technique.

The block diagram of dual slope integrating type DVM is shown in fig. it consists of five blockjs, an op-amp used as an integrator, a zero comparator, clock pulse generator, a set of decimal counters and a block of control logic.

When the switch S_1 is in position 1, the capacitor C starts charging from zero level. The rate of charging is proportional to the input voltage level. The output of the op-amp is given by,

$$V_{out} = -(1/R_1 C) \int_0^{t1} V_{in}\, dt$$

$$\boxed{V_{out} = -(V_{in}\, t_1) / (R_1 C)} \qquad \ldots\ldots\ldots(1)$$

Where, t_1 = Time for which capacitor is charged

V_{in} = Input voltage

R_1 = Series resistance

C = Capacitor in feedback path

After the interval t_1, the input voltage is disconnected and a negative voltage V_{ref} is connected by throwing the switch S_1 in position 2. In this position, the output of the op-amp is given by,

$$V_{out} = -(1/R_1 C) \int_0^{t2} -V_{ref}\, dt$$

Therefore

$$\boxed{V_{out} = -(V_{ref}\, t_2) / (R_1 C)} \qquad \ldots\ldots\ldots\ldots..(2)$$

Subtracting equation (1) from (2),

$$V_{out} - V_{out} = 0 = [-(V_{ref}\, t_2) / (R_1 C)] - [-(V_{in}\, t_1) / (R_1 C)]$$

$$(V_{ref}\, t_2) / (R_1 C) = (V_{in}\, t_1) / (R_1 C)$$

$$V_{ref}\, t_2 = V_{in}\, t_1$$

$V_{in} = V_{ref}\ (t_2/t_1)$ ……(3)

Then the input voltage is dependent on the time period t_1 and t_2 and not on the values of R_1 and C.

This basic principle of this method is shown in fig.

At the start of the measurement, the counter is resetted to zero. The output of the flip- flop is also zero. This is given to the control logic. This control sends a signal so as to close an electronic switch to position 1 and integration of the input voltage starts. It continues till the time period t_1. As the output of the integrator changes from its zero value, the zero comparator output changes its state. This provides a signal to control logic which in turn opens the gate and the counting of the clock pulses starts.

He counter counts the pulses and when it reaches to 9999, it generates a carry pulse and all digits go to zero. The flip-flop output gets activated to the logic level T. this activates the control logic. This sends a signal which changes the switch S_1 position from 1 to 2. Thus - V_{ref} gets connected to op-amp. As V_{ref} polarity is opposite, the capacitor starts discharging. the integrator output will have constant negetive slope as shown in fig. The output decreases linearly and after the interval t_2, attains zero value, when the capacitor C gets fully charged.

At this onstant, the output of zero copmarator changes its gate. This inturn sends a signal to the control logic and the gate gets closed. Thus gate remains open for the period t_1+t_2. the counting operation stops at this instant, the pulses counted by thecounter thus have a direct relation with the input voltage. The counts are then transferred to the readout.

From equation (3) we can write,

$V_{in} = V_{ref}\ (t_2/t_1)$

Let the time period of clock oscillator be T snd digital counter has counted the counts n_1 and n_2 during the period t_1 and t_2 respectively.

Therefore, $V_{in} = V_{ref}\ [(n_2T)/ (n_1T)] = V_{ref}\ (n_2/ n_1)$

Thus the unknown voltage measurement is not dependent on the clock frequency, but dependent on the counts measured by the counter.

The advantages of this technique are:

1. Excellent noise rejection as noise and superimposed ac are averaged out during the process of integration.
2. The RC time constant does not affect the input voltage measurement.
3. The capacitor is connected via an electronic switch. This capacitor is an auto zero capacitor and avoids the effects of offset voltage.
4. The integrator responds to the average value of the input hence sample and hold circuits is not necessary.
5. The accuracy is high and can be readily varied according to the specific requirements.

The only disadvantage of this type of DVM is its slow speed.

3-1/2 and 4-1/2 Digit:

The resolution of digital meters depends on the number of digits used in the display. The three digit display for 0-1 V range can indicate the values from 0 to 999 mV with the smallest increment of 1mV.

Practically one more digit which can display only 0 or 1 is added. This digit is called **half digit** and display is called 3-1/2 digit display. This is shown in fig.9.15.1

In such a display the meter can read the values above 999 upto 1999, to give the overlap between the ranges for convenience. This process is called over-ranging.

In case of 4-1/2 digit display, there are 4 full digits and 1 half digit. The number obtained is from 0-19999. For this operation the time period required for counting operation should be reduced. This can be achieved by changing the frequency of the clock signal. The wave shaping and amplifier circuitry should be more accurate for 4-1/2 digit display. It is necessary to add one more BCD counter, latch, BCD to 7 segment decoder and 7 segment display unit. This resolution of 4-1/2 digit display is better than 3-1/2 digit display while the necessary is 10 times better.

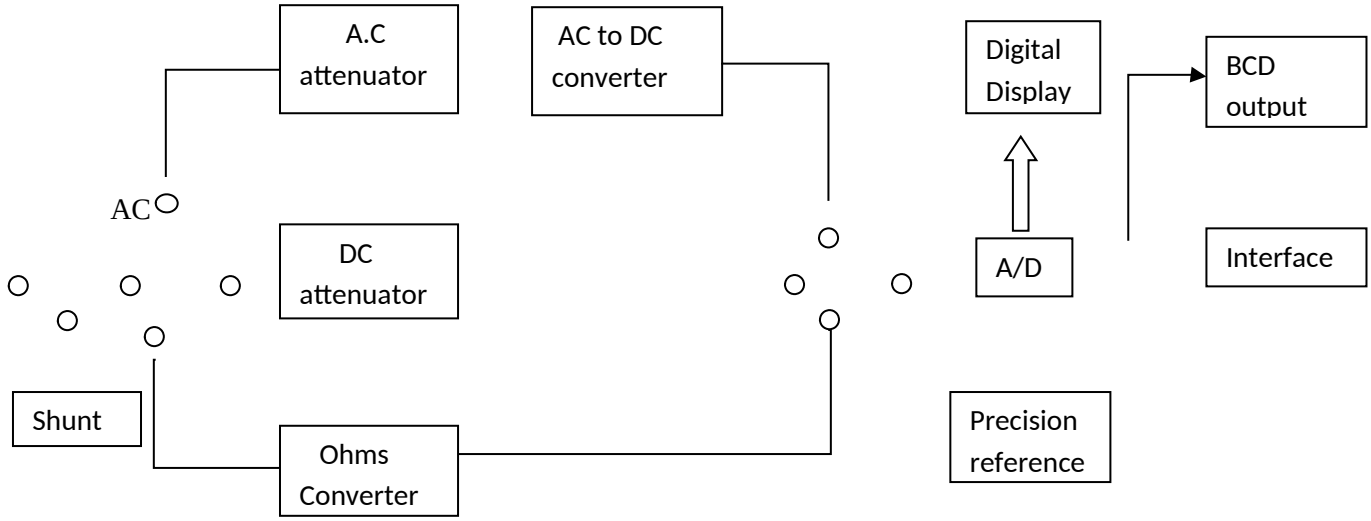
6-1/2 Digit Display:

To increase the resolution and accuracy of measurement, nowadays 6-1/2 digit displays are available. It has six full digits which can display only 0 or 1. This is called half digit. The display is shown in fig.9.15.2

For 1V range, the smallest increment of this display is 1μV and hence measurement accuracy is very high.

Digital Multimeters:

The digital multimeters is an instrument which is capable of measuring ac voltages, dc voltages, ac and dc currents and resistances over several ranges. The basic circuit of a digital multimeter is always a dc voltmeter as shown in fig.



Basic scheme of Digital Multimeter

The current is converted to voltage by passing it through low shunt resistance. The ac quantities are converted to dc by employing various rectifiers and filtering circuits. While for the resistance measurements the meter consists of a precision low current source that is applied across the unknown resistance while gives dc voltage. All the quantities are digitized using analog to digital converter and displayed in the digital form on the diplay. The analog multimeters require no power supply and they suffer less from electric noise and isolation problems but still the digital multimeters have following advantages over analog multimeters:

1) The accuracy is very high.
2) The input impedance is very high hence ther is no loading effect.

3) An unambiguous reading at greater viewing distance is obtained.
4) The output available is electrical which can be used for interfacing with external equipment.
5) Due to improvement in the integrated technology, the prices are going down.
6) These are available in very small size.

The requirement of power supply, electric noise and isolation problems are the two limitations.

The basic building blocks of digital multimeter are several A/D converters, counting circuitry and an attenuation circuit. Generally dual slope integration type ADC is preferred in the multimeters. The single attenuator circuit is used for both ac and dc measurements in many commercial multimeters. The block diagram of a digital multimeter is shown in fig

As mentioned above basically it is a dc voltmeter. In order To measure unknown currents, current to voltage converter circuit implemented. This is shown in fig

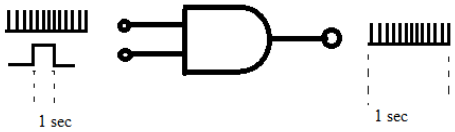
The unknown current is applied to the summing junction $\sum i$ of op-amp at the input of the op-amp. As input current of op-amp is almost zero, the current I_R almost same as I_i . This current $I_{R\ causes}$ a voltage drop, which is proportional to the current to be measured. This voltage drop is the analog input to the analog to digital converter, thus providing a reading that is proportional to the unknown current.

In order to measure the resistance, a constant current source is used. The known current is passed through the unknown resistance. The voltage drop across the resistance is applied to analog to digital converter hence providing the display of the values of the unknown resistance. To measure the ac voltages, the rectifiers and filters are used. The ac is converted to dc and then applied to the analog to digital converter.

In addition to the visual display, the output from the digital multimeters can also be used to interface with some other equipment.

Principle of Digital Frequency Counter:

The signal waveform whose frequency is to be measured is converted into trigger pulses and applied continuously to one terminal of an AND gate. To the other terminal of the gate, a pulse of 1sec is applied as

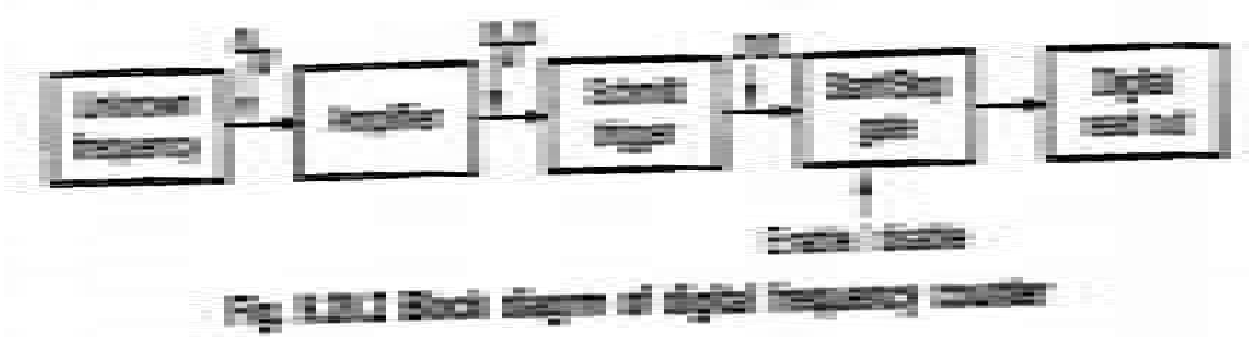


Principle of Digital Frequency Meter

shown in the fig. the number of pulses counted at the output terminal during period of 1sec indicates the frequency.

The signal whose frequency is to be measured is converted to trigger pulses which are nothing but train of pulses with one pulse for each cycle of signal. At the output terminal if AND gate, the number of pulses in a particular interval of time are counted using an electronic counter. Since each pulse represents the cycle of the unknown signal, the number of counts is a direct indication of the frequency of the signal which is unknown. Since electronic counter has a high speed of operation, high frequency signals can be measured.

The block diagram of digital frequency counter is as shown in fig.



The signal waveform whose frequency is to be measured is first amplified. Then the amplified signal is applied to the Schmitt trigger which converts input signal into a square wave with fast rise and fall times. This square wave is then differentiated and clipped. As a result, the output from the Schmitt trigger is the train of pulses for each cycle of the signal. The output pulses from the Schmitt trigger are fed to a START/STOP gate. When this gate is enabled, the input pulses pass through this gate and are fed directly to the electronic counter, which counts the number of pulses. When this gate is disabled, the counter stops counting the incoming pulses. The counter displays the number of pulses that have passed through it in the time interval between start and stop. If this interval is known, the unknown frequency can be measured.

Basic Circuit of Digital Frequency Meter:

The basic circuit if digital frequency meter used for the measurement of frequency consists two R-S flip flops. The basic circuit for measurement of frequency is as shown in the fig.

The output of unknown frequency is applied to the Schmitt trigger which produces positive pulse at the output. These are counted pulses present at A of the main gate. The time base selector provides positive pulses at B of the START gate and STOP gate, both.

Initially FF-1 is at LOGIC 1 state. The voltage from Y output is applied to A of the STOP gate which enables t his gate. The LOGIC 0 state of the output Y is applied to input A of START gate which disables this gate.

When STOP gate enables, positive pulses from the time base pass through STOP gate to S input of FF-2, setting FF-2 to LOGIC-1 state.

The LOGIC 0 level of Y of FF-2 is connected to B of main gate, which confirms that pulses from unknown frequency source can't pass through the main gate.

By applying a positive pulse to R input of FF-1, the operation is started. This changes states of the FF-1 to Y=1andY=0. Due to this, STOP gate gets disabled, while START gate gets enabled. The same pulse is simultaneously applied to all decade counters to reset all of them, to start new counting.

With the next pulse from the time base passes through START gate resetting FF-2 and it changes state from LOGIC 0 to LOGIC 1. As Y changes from 0 to 1, the gating signal is applied to input B of the main gate which enables the main gate.

Now the pulses from source can pass through the main gate to the counter. The counter counts pulses. The state of FF -1 changes from 0 to 1 by applying same pulse from START gate to S input of FF-1. Now the START gate gets disabled, while STOP gate gets enabled. It is important that the pulses of unknown frequency pass through the main gate to counter till the main gate is enabled.

The next pulse from the time base generator passes through STOP gate to S of FF-2. This sets output back to 1 and Y=0. Now main gate gets disabled. The source supplying pulses of unknown frequency gets disconnected. In between this pulse and previous pulse from the time base selector, the numbers of pulses are counted by the counter. When the interval of time between two pulses is 1 second, then the count of pulses indicates the frequency of the unknown frequency source.

Digital Tachometer:

The digital tachometer is used to measure speed of a motor. The technique used for the measurement of a speed of a rotating shaft of a running motor is same as that used in the conventional frequency counter. But in conventional frequency counter, the gate pulses are obtained in accordance with thee Schmitt trigger output while in the digital tachometer the gate period is selected in accordance with the R.P.M calibration.

A typical schematic diagram of digital tachometer is shown in fig.

Consider that the revolution per minute of a shaft be R. Assume that the number pulses produced in one revolution of the rotating shaft be P. Then in one minute the number of pulses from the revolution pick up can be calculated as R * P. Thus the frequency of the signal is given by [R*P /60]. Suppose the gate period is G measured in second, then the pulses counted are [R*P /60]. Now the direct reading is possible in rpm if only the gate period is [60/P] and the pulses counted by the counter are R i.e. [R*P*(60/P)]/60=R.