PART-B
ESSAY QUESTIONS WITH SOLUTIONS

4.1 INTRODUCTION

Q9. What are the salient features of 80386 microprocessor?

Ans:

The important salient features of 80386 microprocessor are,

1. The 80386 processor is capable of running the applications of 8086 under protected mode.
2. The 80386 microprocessor is compatible with its earlier versions i.e., 8086, 8088, 80186, 80188 and 80286 chips.
3. The 80386 allows the programmers to switch between different operating systems such as PC-DOS and UNIX.
4. The 80386 is capable of addressing upto 4 Gbytes physical memory.
5. It can function with 7 different data types such as bit, byte, word, double word, pword, quadword and tenbyte becaue o built in virtual memory management circuitry and protection circuitry.
6. The total number of segments supported by 80386 CPU are 16384 (16K) resulting in an overall virtual memory of 6 terrabytes.
7. The 80386 processor operates in two modes i.e., real mode and protected mode or virtual 8086 mode. In real mode, functions as a fast 8086 or real mode 80286, whereas in protection mode, it serves operations such as paging, virtu addressing, multilevel protection, multitasking and debugging.
8. The 80386 contains an on-chip address conversion cache.
9. The 80386 has pipelined architecture which permits simultaneous instruction fetching, decoding, execution and memory management. It can execute about 3-4 million instructions per second.
10. It has low cost and low power versions, which are widely used in many applications.
11. It is usually available in a 132-pin grid array package with 20 and 33 MHz versions.

Q10. With a neat block diagram, explain the architecture of 80386 microprocessor.

Model Paper-I,

Ans:

The architecture of 80386 is divided into three sections which is illustrated in figure (1).

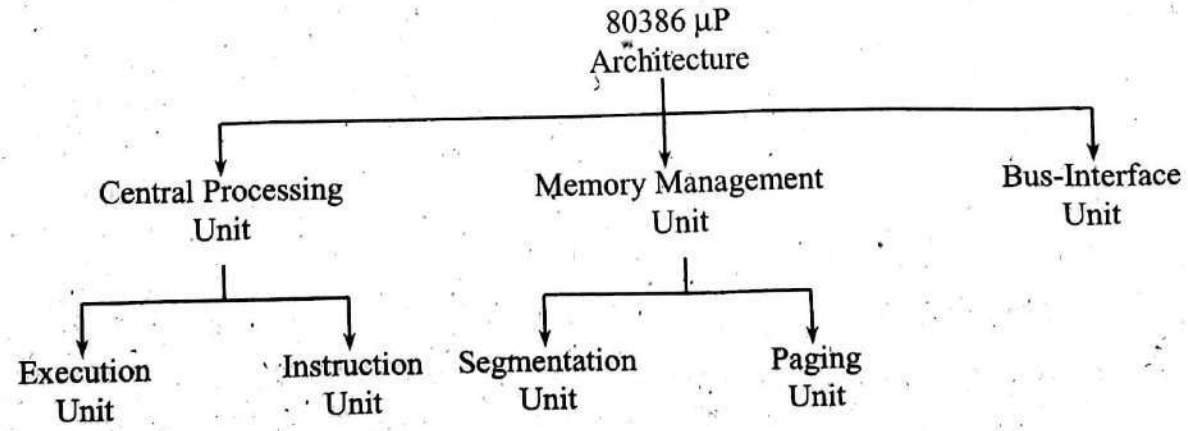


Figure (1)

The internal architecture of 80386 microprocessor is as shown in figure (2).

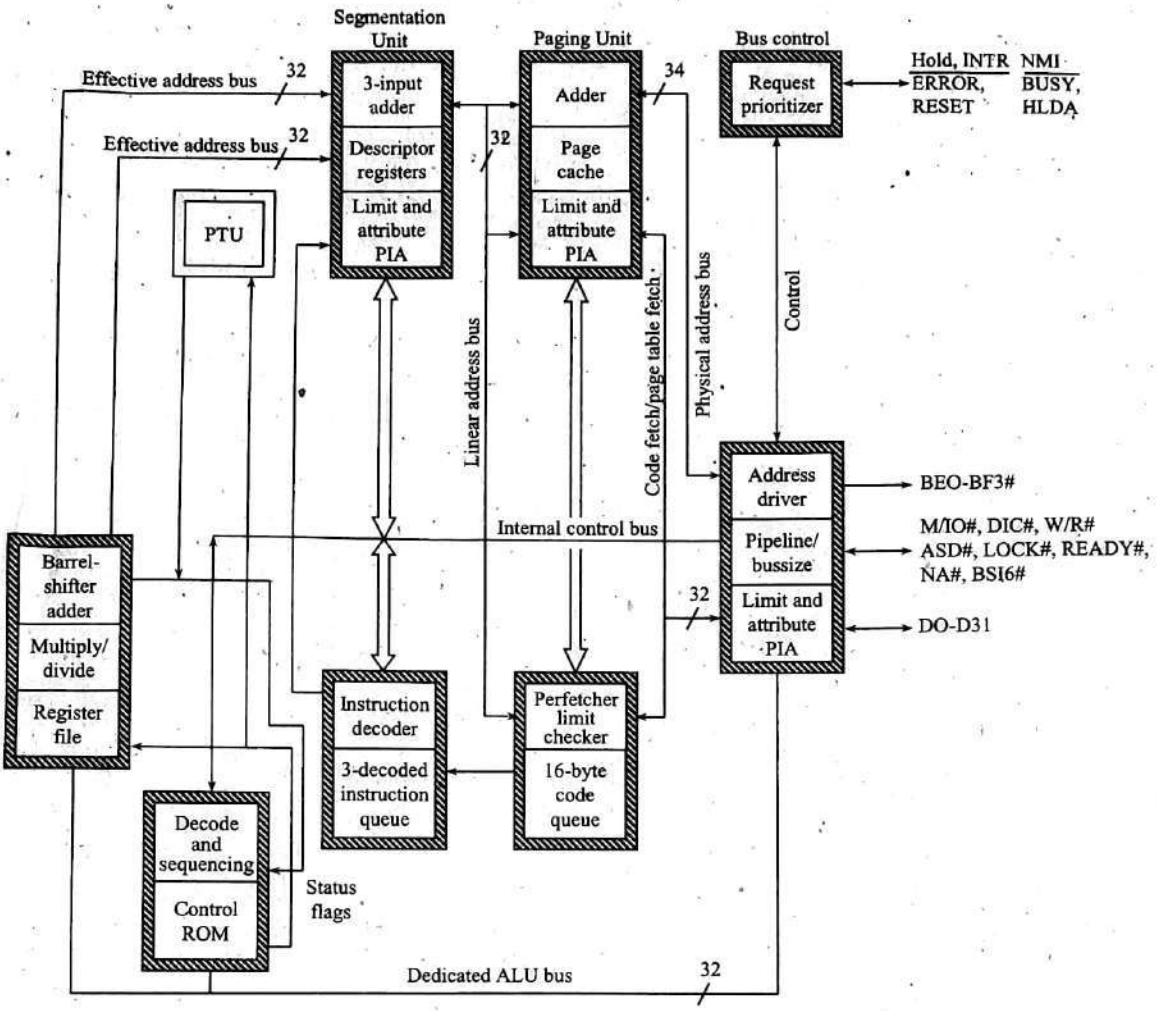


Figure (2): Block Diagram of 80386

Execution Unit: The execution unit of CPU handles data or reads the decoded instruction and calculates its offset address by using eight general purpose and eight special purpose registers. It includes,

1. **Control Unit** – It contains stored microcode in ROM for instructions and flag register. It produces necessary internal control signals based on the decoded opcodes..
2. **Data Unit** – It contains 64-bit barrel shifter, multiply/divide unit and eight general purpose registers. It performs the operations required for control unit.
3. **Protection Test Unit (PTU)** – Based on the micro code, it monitors any violations in segmentation.

Instruction Unit

1. **Instruction Prefetch Unit:** In this unit of CPU, the instructions are fetched and stored in the 16- byte code queue. This operation is performed only when the bus is free.
2. **Instruction Decode Unit:** In this, the prefetched instruction in read and decoded and then queued in the decode unit.

Segmentation Unit: The segmentation unit of memory management unit(MMU) uses segment and offset addresses to share or relocate the data or code. In real address mode, it calculates the addresses as in 8086 or 80286. In protected virtual address mode, it calculates a 32-bit linear address by using offset, selector and descriptor.

Segmentation unit protects the system code by isolating it from application program using a four level mechanism. The maximum allowable size of segments in this unit is 4 Gbytes.

Paging Unit: Paging unit of MMU is also considered as a segmentation unit with each segment divided into pages. It contains physical memory as pages of each 4kbyte. If paging unit is enabled, it converts 32-bit linear address to 32-bit physical address otherwise it uses the linear address as physical address.

Control and Attribute PLA: It is used to monitor each page that contains the paging information of the task.

Limit and Attribute PLA: It is used to verify the segment limits and their attributes to avoid invalid access to code or data.

Bus Control Unit: It controls various bus requests by using a prioritizer.

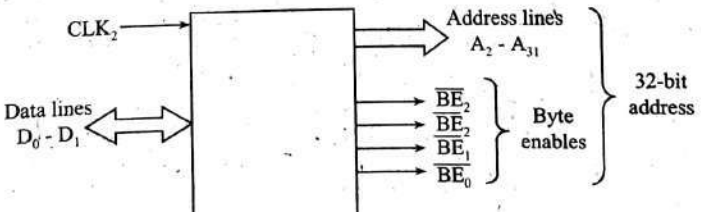
Address Driver: It is used to drive the bus enable and address signals.

Pipeline and Dynamic Bus Sizing Units: It is used to handle the control signals.

Data Buffer: It is used to interface internal bus with system bus.

Q11. Write about signal description of 80386 processor.

Ans: The modified pin diagram of 80386 microprocessor is as shown in figure below.



4.2 SPECIAL PURPOSE REGISTERS

Q14. Draw and discuss the register set of 80386 and explain the function of each of the registers in brief.

Model Paper-III, Q5(b)

Ans:

The 80386 processor has seven types of register sets. They are,

(i) General purpose registers

(ii) Segment registers

(iii) Flag registers and instruction pointer

(iv) Segment descriptor registers

(v) Control registers

(vi) System address registers and system segment registers

(vii) Debug and test registers.

(i) General Purpose Registers

80386 architecture contains 8 general purpose registers. Each register is of 32-bit and can also be used either as 8-bit or 16-bit registers. Figure (1) shows the general purpose registers set of 80386.

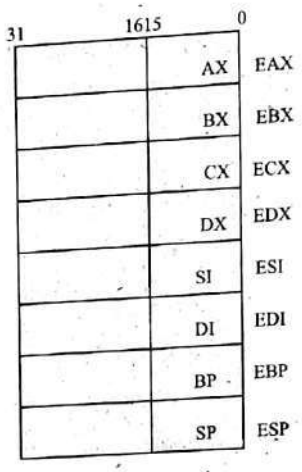


Figure (1): General Purpose Registers

Basically in 80386 processor a 32-bit general purpose register is referred as extended register and is denoted by a register name with prefix E. For example, a 32-bit register related to AX is represented by EAX, similarly EBX, ECX, ESI etc., for BX, CX and SI respectively. AX denotes the lower bits of 32-bit register EAX. AH and AL each represent 8-bit of 16-bit AX. Moreover BX, CX and DX also have their 8-bit, 16-bit and 32-bit register representations.

80386 supports four index registers which can be used either as 16-bit or 32-bit registers. The 16-bit index registers are BP, SP, SI and DI whereas 32-bit index registers are EBP, ESP, ESI and EDI. All these registers perform same functions as in 80286.

(ii) Segment Registers

80386 architecture has six segment registers i.e., CS, SS, DS, ES, FS and GS. Figure (2) shows the segment registers.

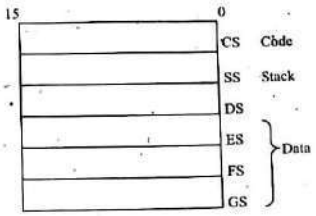


Figure (2): Segment Registers

These segment registers perform same functions as in 80286.

(iii) Flag Registers and Instruction Pointer

80386 architecture contains a 16-bit Instruction Pointer (IP) which can also be used as 32-bit instruction pointer (EIP). Figure (3) shows the format of IP and flag registers.

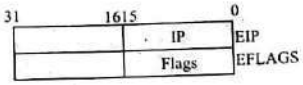


Figure (3): Instruction Pointer and Flag Register

80386 architecture contains a 32-bit flag register. The lower 15 bits i.e., D_0 - D_{14} are same as 80286 flag register and also perform same operation. The bit 'D_1' is always set at '1' and the bits. D_3, D_5, D_{15} and D_{18} - D_{31} are reserved for future use. In this flag register only two bits are new when compared them with 80286. They are *VM*(at D_{17}) and *RF* (at D_{16}) flags. Figure (4) shows the flag register of 80386.

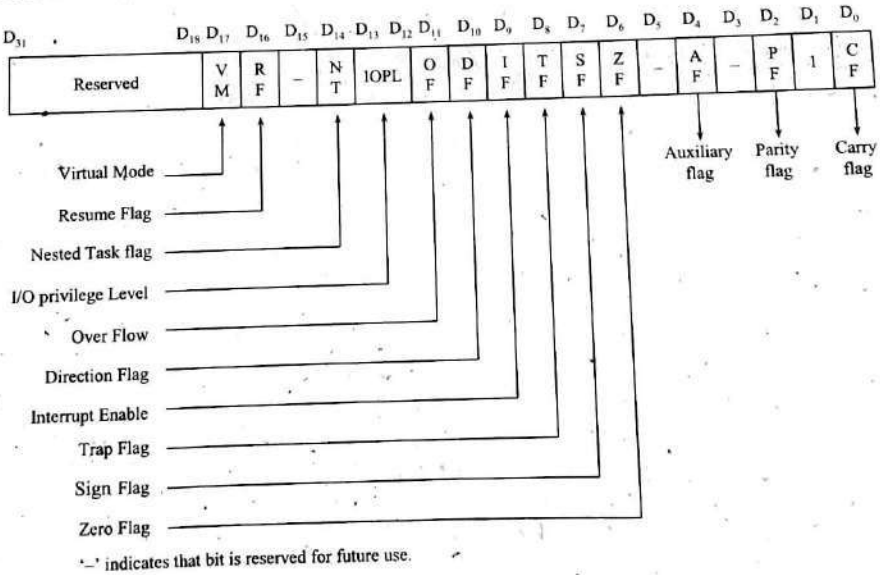


Figure (4): Flag Register of 80386

Virtual Mode (VM) Flag: When 80386 operates in protected mode then only it is possible to set the *VM* flag, if *VM* is set to 1 (i.e., *VM* = 1) then 80386 enters virtual 8086 mode within the protected mode. In this mode, an exception 13 is generated on the execution of privileged instruction. Task switch operations and IRET instruction are used to set *VM* flag.

Resume Flag (RF): The Resume Flag (RF) comes into picture only when debug register breakpoints are in use. At the initial stage of every instruction cycle, RF is checked. If RF = 1, then debug fault is ignored during instruction cycle. RF resets automatically after every successful execution of instructions except for IRET and POPF instructions. However, it is not cleared automatically after execution of instructions like JMP, CALL and INT.

IOPL: IOPL flags are used to indicate the privilege level of current I/O operations.

(iv) Segment Descriptor Registers

80386 processor has six 73-bit segment descriptor registers corresponding to six segment registers. These registers are used internally to store the descriptor information such as, attributes, limit and base addresses and also these are not available for programmers. These registers are mapped with the segment registers and loaded automatically only when the corresponding segment registers loaded with selectors. Each 73-bit segment descriptor register comprises of 32-bit base address, 32-bit base limit and 9-bit attributes as shown in figure (5).

Segment registers		Descriptor registers (loaded automatically)						
15 0		Physical base	Address	Segment Limit		Attributes	Other segment from descriptor	
Selector	CS –						–	–
Selector	SS –					–	–	–
Selector	DS –					–	–	–
Selector	ES –					–	–	–
Selector	FS –					–	–	–
Selector	GS –					–	–	–

Figure (5): 80386 Segment and the Corresponding Descriptor Registers

(v) Control Registers

80386 architecture contains four 32-bit control registers i.e., CR_0, CR_1, CR_2 and CR_3. The control registers CR_0, CR_2 and CR_3 are used to keep the global machine status independent of executed task. However, the register CR_1 is reserved for future use. These registers can be accessed by the load and store instructions.

(vi) System Address Registers and System Segment Registers

80386 processor has four descriptor tables. They are,

(a) Global Descriptor Table (GDT)

(b) Interrupt Descriptor Table (IDT)

(c) Local Descriptor Table (LDT)

(d) Task State Segment [TSS] Descriptor

The addresses of four descriptor tables and corrosponding segments are stored in system address registers and system segment registers. The system address registers are GDTR [Global Descriptor Table Registor] and IDTR [Interrupt Descriptor Table Registor]. Whereas the system segment registers are LDTR[Local Descriptor Table Register] and TR [Task Register].

(vii) Debug and Test Registers

80386 architecture supports a set of 8 debug registers and two test registers. Figure (6) shows the sets of debug and test registers. The debug registers are DR_0 - DR_7 out of these registers two are reserved for future i.e., DR_4 and DR_5. The four registers i.e., DR_0 - DR_3 are used for hardware debugging and last two registers i.e., DR_6 - DR_7 are used to keep the breakpoint control information and breakpoint status.

The two test registers i.e., test control register (TR_6) and test status register (TR_7) are used for page caching.

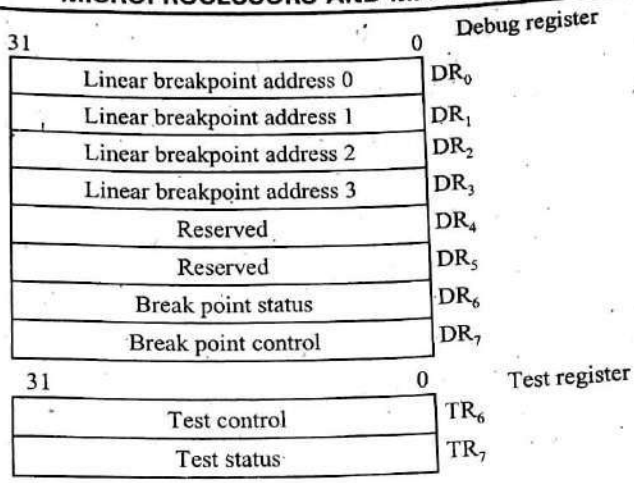


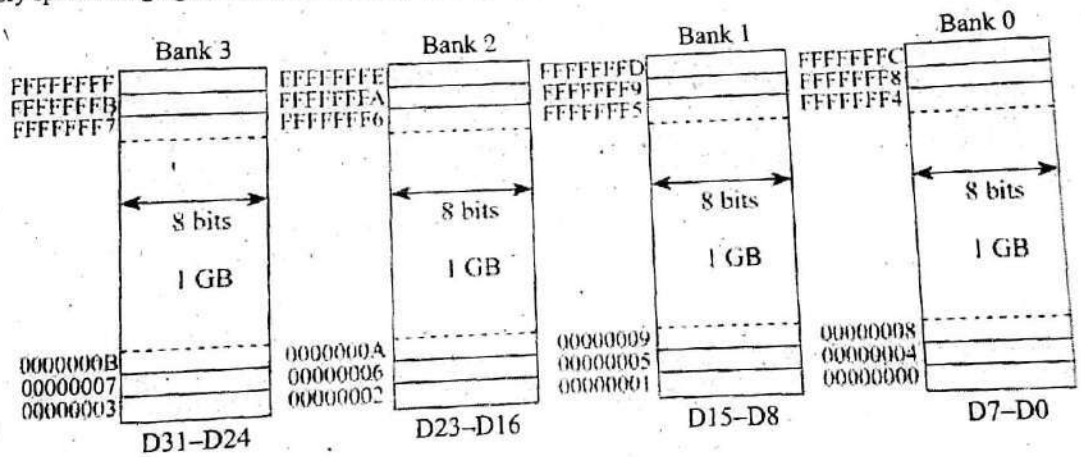
Figure (6): Debug and Test Registers

4.3 MEMORY ORGANIZATION

Q15. Explain physical memory organization in 80386.

Ans:

The physical memory address space of 80386 microprocessor is 4 GB with an address range 00000000H – FFFFFFFFH. This memory space is segregated into four memory banks, each of 8-bits wide holding 1GB memory as shown in figure.



Figure

The address range of the four memory banks is mentioned in table.

Bank	Address Range
0	00000000H – FFFFFFFCH
1	00000001H – FFFFFFFDH
2	00000002H – FFFFFFFEH
3	00000003H – FFFFFFFFH

Table

The data i.e., bytes or words in these memory banks can be accessed through bank enable signals ($\overline{BE3}$, $\overline{BE2}$, $\overline{BE1}$ and $\overline{BE0}$).

4.4 PROGRAMMING CONCEPTS, MOVING TO PROTECTED MODE, VIRTUAL MODE, MEMORY PAGING MECHANISM

Q16. With a neat sketch, explain the addressing in protective mode of 80386.

Ans:

Protected Mode of 80386: In this mode, additional instructions, addressing modes and all the capabilities of 80386 are used. The drawback of real addressing mode can be overcome in this mode. It can address almost 4 GB of physical memory and 64 TB of virtual memory per task.

Addressing: Figure (1) shows the schematic protected mode addressing.

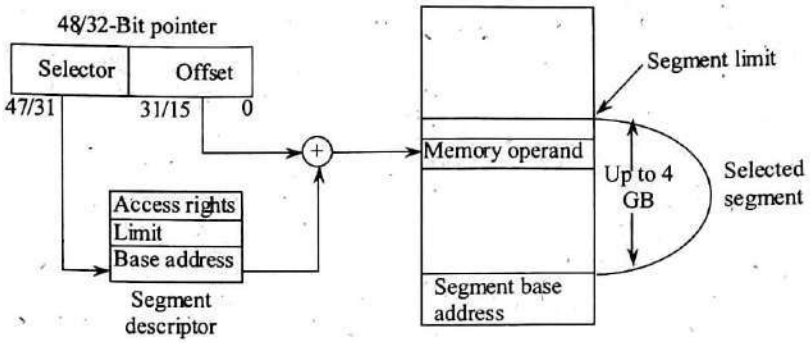


Figure (1): Protected Mode Addressing Without Paging Unit

The linear address is calculated by adding the offset address with segment base address, in order to use this address as physical address, the paging unit is disabled. If the paging unit is enabled then, the linear address is automatically converted into physical address.

Figure (2) shows the paging unit enabled in protected mode addressing.

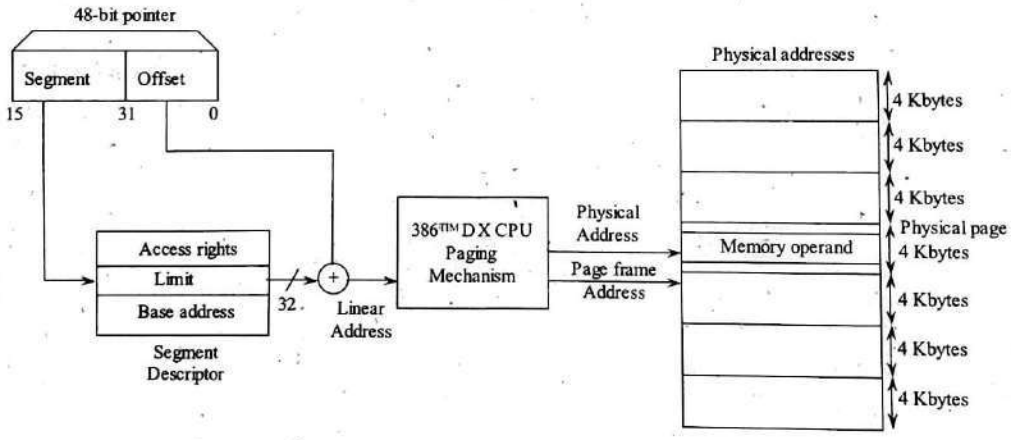


Figure (2): Paging Unit Enabled in Protected Mode Addressing

By using the control of segmentation unit, the paging unit operations are performed. Each segment may be of 4 kB size.

Q17. Write a short note on virtual 8086 mode of 80386. Model Paper-III, Q5(a)

Ans: The 80386 enters from protected mode into virtual mode when VM bit of flags register is set to '1'. The virtual mode is employed to execute the 8086 programs. These programs can also be executed using real mode. But, reset operation should be done to leave the protected mode if once it has entered the protected mode from the real mode.

The virtual 8086 programs are executed simultaneously on virtual machines. A virtual machine consists of software and hardware and every machine has 1 MB addressing space. This 1 MB addressing space lies anywhere in the memory. In the TSS of virtual task, the processor registers are maintained via their corresponding entries. Like real mode, the size of registers are defaulted to 16-bits. With common constraints, override prefixes can be employed to permit 32-bit registers and addressing modes. The concept of virtual machines running on the pentium is as shown in figure below.

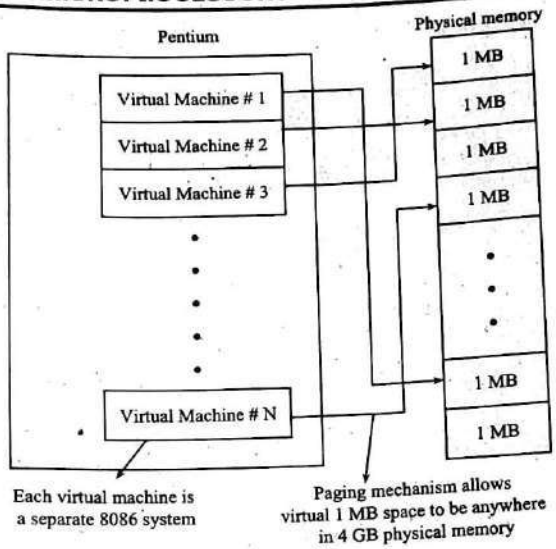


Figure: Virtual Machines on Pentium

Address generation in virtual mode is same as real mode.

Q18. Discuss the paging mechanism of 80386 in detail.

Model Paper-II, Q5(b)

Ans:

Paging in 80386 Processor: Paging is a memory management technique that is employed in virtual memory multitasking operating systems. In this technique, the physical memory is divided into fixed size pages that contains portions of program and data.

The main advantage of this technique is the reduction in memory requirement of the task, because it is not necessary that complete task code be in the physical memory but only few pages are to be available in the physical memory, thus relinquishing the available memory to the other tasks.

The paging in 80386 is accomplished by a paging unit present in it. It derives the physical address of a page from the available linear address in two levels.

The paging unit defines three components for every task.

1. Page directory
2. Page tables
3. Page itself.

The base address of the page segment is store in a register called page descriptor base register.

1. Page Directory

The page directory has a maximum size of 4 kbytes and the size of each directory entry four bytes, hence a total of 1024 entries are valid in the directory. Figure (1) shows a directory entry, the upper 10 bits give the index address that points to a page table.

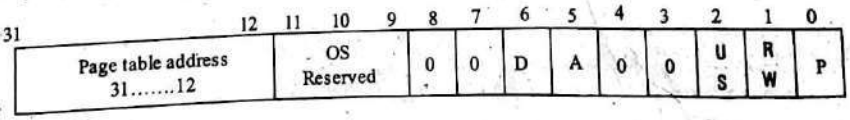


Figure (1): Page Directory Entry

2. Page Table

A page table is also of 4 Kbytes in size and it contains a maximum of 1024 entries. Figure (2) shows a page table entry, it contains of starting address of page (Upper 20 bit) and the ending address of a page (Lower 12).

31 ... 12	11 10 9	8	7	6	5	4	3	2	1	0
Page frame address 31.....12	OS Reserved	0	0	D	A	0	0	U S	R W	P

Figure (2): Page Table Entry

The functions of each bit in above two entries are same.

The '*P*' bit decides if the entry can be used in address translation or not. If $P = 1$ it can be used, else if $P = 0$ it cannot be used.

The *A* bit (accessed bit) is 1, denotes that the accessing of page is permitted else if it is 0 the page cannot be accessed.

The *D* bit (dirty bit) is mode 1 to enable the write operate to the page. It is undefined for page directory entries.

The U/S bit (User/Supervisor) and R/W bit (Read/Write) provides protection. The combination of these bits define protection under the 4 level protection model as shown below.

U/S	R/W	Permitted for Level 3	Permitted for Level 0,1,2
0	0	None	Read/Write
0	1	None	Read/Write
1	0	Read only	Read/Write
1	1	Read-Write	Read/Write

Table: Four Level Protection Mode

Figure (3) illustrates the block diagram of a paging unit in 80386 processor.

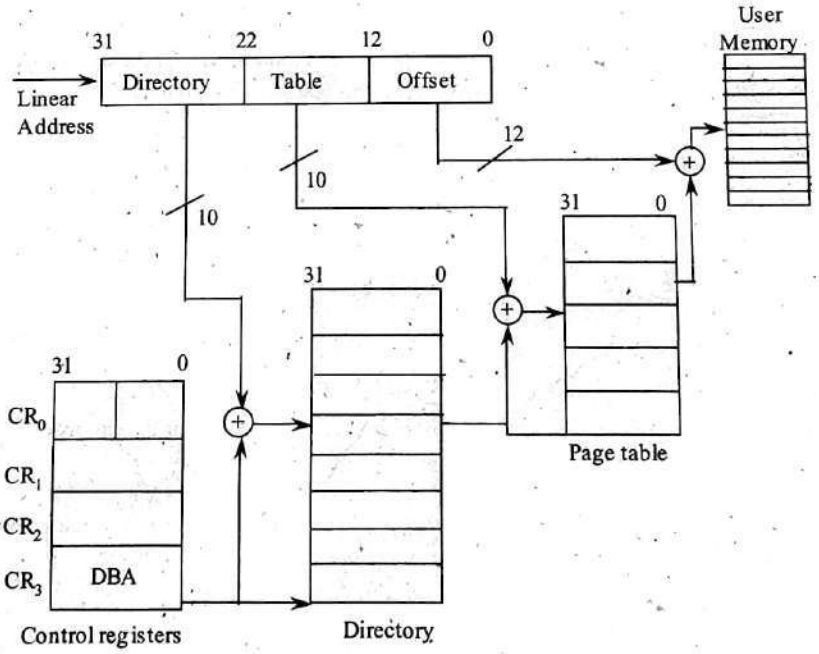


Figure (3): Paging Operation of 80386 Processor

DBA is the physical director base address which added together with the directory index address points to a particular directory.

The address present in the directory location added with table index address points to a particular page table. The address in the selected page table on adding with OFFSET address points to the particular page in the user memory.

4.5 ARCHITECTURAL DIFFERENCES BETWEEN 80386 AND 80486 MICROPROCESSORS

Q19. Compare/contrast the features of 80386 and 80486 processors. Model Paper-I, Q5(b)

Ans:

The comparison between the features of 80386 and 80486 processors is mentioned below:

S.No.	Parameter	80386	80486
1.	Year of introduction	It was introduced in 1986	It was introduced in 1989
2.	Size	It is a 32-bit μp.	It is a 32-bit μp.
3.	Data bus	It consists of 32-bit data bus.	It consists of 32-bit data bus.
4.	Address bus	It consists of 32-bit address bus.	It consists of 32-bit address bus.
5.	Memory space	It has 4 GB of physical memory space and 64 TB. of virtual memory space.	It has 4GB of physical memory space and 64 TB of virtual memory space.
6.	Cache memory	It does not contain cache memory.	It contains 8 kB of cache memory.
7.	Pipelining	It supports pipelining process.	It supports pipelining process.
8.	Operating modes	It operates in real, protected and virtual 8086 modes.	It operates in real, protected and virtual 8086 modes.
9.	Clock frequency	The internal clock rating is 16 or 20 or 25 or 33 MHz.	The internal clock rating is 25 or 33 or 50 MHz