PART-B

ESSAY QUESTIONS WITH SOLUTIONS

5.1 ARCHITECTURE, HARDWARE CONCEPTS

Q12. List the features of 8051 family of microcontrollers.

Ans: The following are some of the features of 8051 family of microcontrollers.

1. 8051 microcontrollers have 4096 bytes of internal program memory.
2. They have 128 bytes of internal data memory.
3. 8051 microcontrollers possess four register banks.
4. 128 user-defined software flags are available in 8051 microcontrollers.
5. They possess one microsecond instruction cycle with 12 MHz crystal.
6. 8051 microcontrollers have 32 bidirectional I/O lines organized as four 8-bit ports.
7. They consist multiple mode, high-speed programmable serial port.
8. 8051 microcontrollers have 16-bit timers/counters.
9. They possess two-level prioritized interrupt structure.
10. 8051 microcontrollers support full depth stack for subroutine return linkage and data storage.
11. They have direct byte and bit address abilities.
12. 8051 microcontrollers support signal overflow detection and parity computational features.

Q13. Explain the architecture of 8051 with its diagram. Model Paper-I, Q6(a)

(or)

Explain in detail about the architecture of 8051 microcontroller with a neat diagram.

Ans: Figure (1) shows the functional block diagram of 8051 microcontroller.

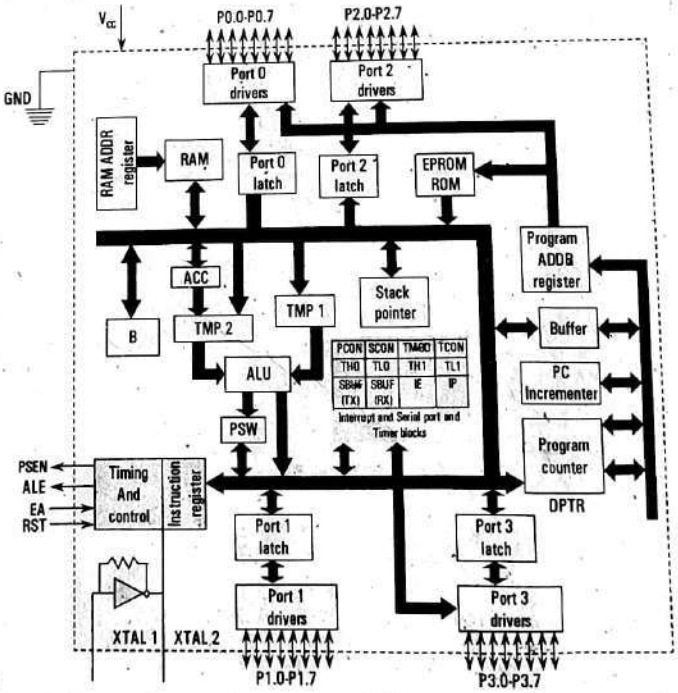


Figure (1): Block Representation of 8051

The individual blocks of 8051 microcontroller are discussed below.

Program Counter (PC): PC is a 16-bit register, that holds program memory address of currently fetching instruction. It is capable of addressing 64 k bytes of code.

PC Incrementer: This is a 16-bit register which keeps incrementing the address in accordance with the program flow. It is used to facilitate PC to be used for addressing modes.

DPTR: It consists of two 8-bit registers, DPH and DPL. It is used to hold a 16-bit address. DPTR holds data in indirect addressing mode.

Accumulator (A): It is an 8-bit register that stores one of the operands and its immediate results of ALU operation.

B Register: It is an 8-bit register that holds second operand while performing ALU operations. B register is used during multiply and divide operations along with A register.

ALU (Arithmetic and Logical Unit): It performs arithmetic operations like addition, subtraction, multiplication, division and logical operations like AND, OR, NOT, EXOR, etc.

PSW (Program Status Word): PSW contains four mathematical or math flags, one user program flag and two register select bits as shown in figure (2).

7	6	5	4	3	2	1	0
CF	AC	F0	RS1	RS0	OV	F1	P

Figure (2)

Carry Flag (CF): After performing an arithmetic or logical operation, if there is a carry from MSB then CF is set, otherwise cleared. It is used in arithmetic, jump, rotate and boolean instructions.

Auxiliary Carry Flag (AC): After an arithmetic or logical operation if there is a carry or borrow from 3rd bit to 4th bit then AC flag is set, otherwise cleared. It is used for BCD arithmetic operations.

Overflow Flag (OV): This flag is set whenever the result of a signed number operation is too large causing the higher order bit to flow into the sign bit.

Parity (P): This flag is set if register A contains odd number of ones and cleared if register A has even number of ones.

User Flag (F0): This flag is set/cleared by software as a user defined status flag. User flag is also called general purpose flag.

RS1	RS0	Register bank	Address
0	0	0	00-07 H
0	1	1	08-0F H
1	0	2	10-17 H
1	1	3	18-1F H

Table: Register Select Bits

Flag F1: *Flag 1 of the user.*

Stack Pointer: *Stack is a section of RAM used by the CPU to store information temporarily. Stack pointer is 8-bit wide. The address held in the stack pointer is the location in the internal RAM where the last byte of data was stored by stack operation.*

Temporary Register - Temp 1 and Temp 2: Temp1 and Temp 2 registers are used during comparisons and in certain other operations. These operations use the contents of registers but do not modify them.

Timing and Control: All operations are performed in synchronous with the clock pulse. The control unit generates control signals like ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$.

ALE: While accessing external memory, the low address byte is latched through this pin.

$\overline{PSEN}$: It is an active low program strobe enable used for reading the contents of external program memory.

$\overline{RD}$: It is an active low read signal used for reading the contents of external data memory.

$\overline{WR}$: It is an active low write signal used for writing the contents to external data memory.

IR (Instruction Register): It holds the opcode of current instruction.

Program Address Register: This is a 16-bit register which holds the address of the code to be accessed. The PC holds the address for application to the address bus pins and it also outputs the address for the code (or) data. There, the program address register finds its move instruction.

RAM Address Register: Similar to program address register, it holds the address of the reference data. It finds its use during move instruction.

ROM: It is a read only program memory. The ROM can be a masked ROM, erasable PROM (EPROM) or flash EEPROM.

TMOD (Timer Mode Register): It is an 8-bit register that specifies operation of timer 0 and timer 1 along with their modes.

TCON (Timer Control Register): It is an 8-bit register that stores TF and TR of both timer 0 and timer 1 along with interrupt control bits.

SCON (Serial Control Register): SCON register is an 8-bit register used to program start, stop and data bits of data framing.

PCON (Power Control Register): It contains the flags that differentiates power-on-reset, crown-out-reset, watchdog timer reset and an external $\overline{MCLR}$ reset.

SBUF: It is used for serial transmission and reception.

Q14. List out the available special function registers and their addresses in 8051.

Ans: Special function registers are commonly known as SFRs. The address of special function registers lies in between 80 H and FF H. All the address locations are not used by SFRs. So, the unused address space between 80 H and FF H are reserved and cannot be used by 8051 users. The special function registers and their addresses are mentioned in table below.

Symbol	Name	Internal RAM(Hex)
A	Accumulator	0E0
B	Arithmetic	0F0
DPH	Addressing external memory	83
DPL	Addressing external memory	82
IE	Interrupt enable control	0A8
IP	Interrupt priority	0B8
P0	Input/output port 0 latch	80
P1	Input/output port 1 latch	90
P2	Input/output port 2 latch	A0
P3	Input/output port 3 latch	0B0

(i) **Pin-29 ($\overline{PSEN}$ -Program Store Enable):** $\overline{PSEN}$ is an active low, output control signal. While executing the external program memory, the $\overline{PSEN}$ signal gets activated at every six oscillator periods. The $\overline{PSEN}$ signal serves as the read strobe to the external program memory. This signal causes the external program memory to enable its contents to the 8051.

(ii) **Pin-30 (ALE-Address Latch Enable):** ALE is an active high output signal. While accessing the external memory, this signal is used to latch the lower byte of the address which is time multiplexed with port 2.

(iii) **Pin-31 ($\overline{EA}$ -External Access):** $\overline{EA}$ is an active low signal. When the $\overline{EA}$ pin is high, i.e., $\overline{EA}$ = 1 the 8051 fetches the program instructions from the internal program memory for addresses 0000 H to 0FFF H whereas 8051 fetches the program instructions from the external program memory for addresses 0000 H to FFFF H. When the $\overline{EA}$ pin is low, i.e., $\overline{EA}$ = 0, the 8051 microcontroller fetches the program instructions from external program memory for addresses 0000 H-FFFF H.

5. **Pin-9 (RST-Reset):** The RST pin is used to reset the 8051 microcontroller. In order to reset 8051, a high signal should be applied to this pin for two machine cycles, while the oscillator is running.

Q18. Discuss in detail about parallel I/O ports in 8051 microcontroller and explain how these ports are accessible for specific applications.

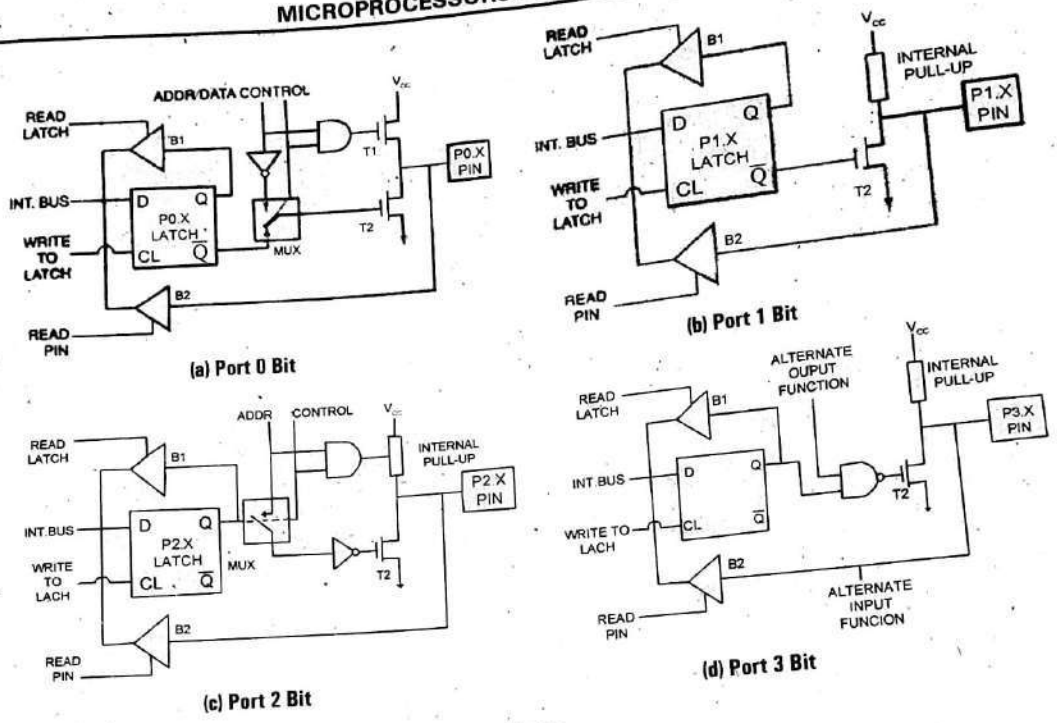
Ans: The 8051 has four bi-directional ports and they are,

1. Port 0 (P0)
2. Port 1 (P1)
3. Port 2 (P2)
4. Port 3 (P3).

Each port consists of a latch, an output driver and an input driver.

The input and output drivers of port 0 and the output drivers of port 2 are used to access the external memory. The lower byte of the external memory address is given by the port 0, which is time multiplexed with the byte being read or written while the port 2 outputs the higher byte of the external memory address. If the address is 16-bit wide i.e., port 0 carries AD_0 to AD_7 multiplexed address and data bus, and port 2 would be outputting the A_8 - A_{15} address line. All the port 3 pins are multifunctionals. Apart from being ports pin, they also serve the functions of various special features such as,

P3.0	RxD	Serial input port
P3.1	TxD	Serial output port
P3.2	$\overline{INT0}$	External interrupt 0
P3.3	$\overline{INT1}$	External interrupt 1
P3.4	T0	Timer0/Counter 0 external input
P3.5	T1	Timer1/Counter 1 external input
P3.6	$\overline{WR}$	External data memory write strobe
P3.7	$\overline{RD}$	External data memory read strobe.



Figure

The above functional diagram shows that each of the four ports consists of a typical bit latch and I/O buffer. Type D flip-flop is used to represent the bit latch. In response to a "write to latch" signal from the CPU, D flip-flop will clock in a value from the internal bus. Along with the response to the "read pin" signal from the CPU; the level of the port pin itself is also placed on the internal bus. Some instructions that read a port, activate the read latch signal and others activate the "read pin" signals.

From the functional diagram it is observed that the output drivers of ports 0 and 2 are switchable to an internal address and address/data bus by an internal control signal for it in external memory access.

Also, if there is a '1' in the P3 bit latch, then the output is controlled by the signal labeled "alternate output function".

5.3 EXTERNAL MEMORY

Q19. Draw and explain the capacities of internal and external program memory and internal and external data memory.

Ans:

Memory organization in 8051 microcontroller is done as follows,

1. Program Memory
   - (i) External program memory
   - (ii) Internal program memory.
2. Data Memory
   - (i) External data memory of 64 k bytes capacity
   - (ii) Internal data memory of 256 bytes capacity.

1. **Program Memory:** Program memory is accessed through $\overline{EA}$ pin.

   (i) If $\overline{EA}$ is high, then internal program memory is accessed till 0FFFH memory location and external program memory is accessed from 1000H to FFFFH memory location.

   (ii) If $\overline{EA}$ pin is low, only external program memory is accessed from 0000H to FFFFH memory locations (64 k). Program memory organization in 8051 as shown in figure (1),

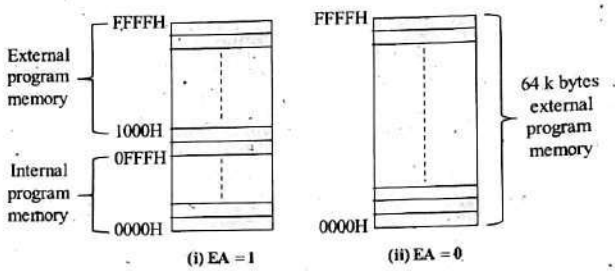


Figure (1): Program Memory

2. **Data Memory:** Data memory organization is as shown in figure (2). The instruction MOVX is used to access external data memory of size 64 k. Here, internal data memory of 256 bytes has two partitions,

   (i) 00H – FFH for internal data RAM (128 bytes)

   (ii) 80H – FFH for special function registers (128 bytes).

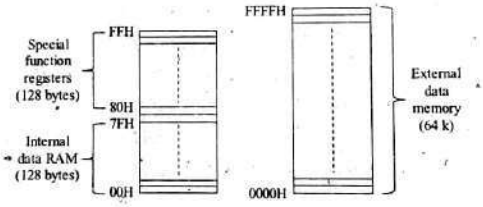


Figure (2): Data Memory Organization

5.4 COUNTERS/TIMERS

Q20. Draw and discuss the formats and bit definitions of the following SFR's in 8051 micro-controller.

(a) TCON

(b) TMOD.

(or)

Explain TCON and TMOD function registers of 8051.

(Refer Only TCON (Timer Control Register) and TMOD (Timer Mode Control)

Ans:

(a) **TCON (Timer Control Register):** This is an 8-bit register. Figure (1) shows the bit assignments for TCON register. The upper four bits are used to store the *TF* and *TR* bits of both timer 0 and timer 1 and lower 4 bits are used for controlling interrupt bits.

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Figure (1): Timer Control Special Function Register

pulses from external ... cleared to 0 by program it is used as a timer.

M0, M1: Mode Select Bits. These bits are used to select the timer mode. There are three modes. Mode 0 is a 13-bit timer, mode 1 is a 16-bit timer and mode 2 is an 8-bit timer.

Q21. Explain with waveforms different modes of counter/timer in 8051.

Ans:

Modes of Counter/Timer in 8051

Mode 0: In the mode 0 the timer register is configured as a 13-bit register. As the count rolls from all '1's to all '0's it sets the timer interrupt flag *TF*1. The counted input is enabled to Timer/Counter. When *TR*1 = 1 and either gate = 0 or $\overline{INT1}$ = 1. The 13-bit register consists of all 8-bits of *TH*1 and the lower 5-bits of *TL*1. It holds values between 0000h to 1FFFh in TH1 and *TL*1. The upper 3-bits of *TL*1 are indeterminate and should be ignored. When the timer reaches its maximum value 1FFFH it comes to initial value 0000 and *TF* is raised.

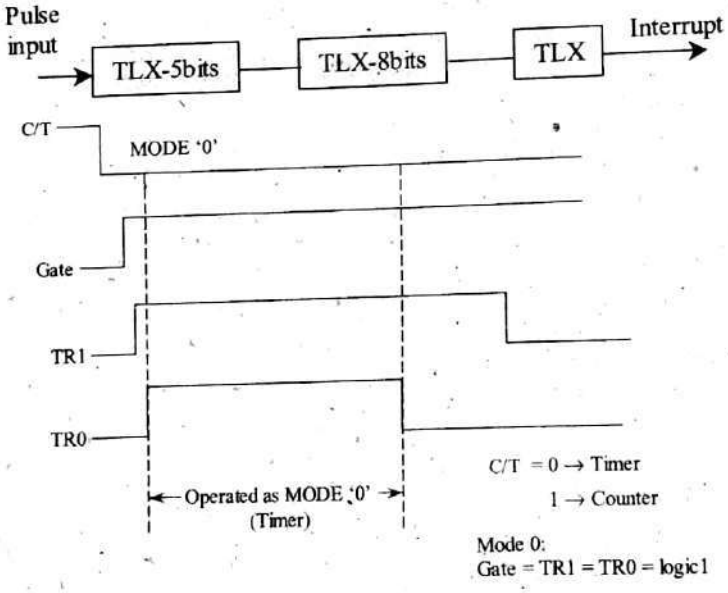
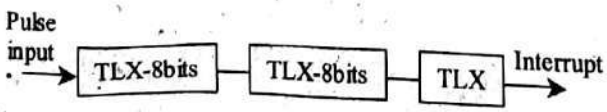


Figure (1)

Mode 1: This mode is same as mode 0 except that the timer register is being run with all 16-bits. Therefore values of 0000 to FFFFH can be loaded into the timer's register *TL* and *TH*. Once it is loaded, the timer must be started. The timer starts counting and continues till it reaches its limit of FFFFH. When it moves from FFFF to 0000, it sets the timer flag once *TF* =1 the timer is stopped.



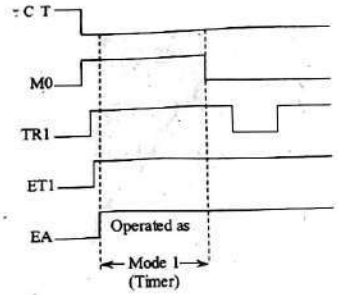


Figure (2)

$C/\overline{T} = 0 \rightarrow$ Timer

$= 1 \rightarrow$ Counter

Mode 1:

M0 = TR1 = ET1 = EA = logic 1

Mode 2: It is an 8-bit timer, therefore it allows only values of 00 to FFH to be loaded into the timers register *TH*. After *TH* is loaded with the 8-bit value, then the timer must be started.

After the timer is started, it starts count up by incrementing the *TL* register. It counts up till it reaches its limit of FFH. When it moves from FFH to 00 it sets the timer flag. *TL* is reloaded automatically with the original value kept by the *TH* register.

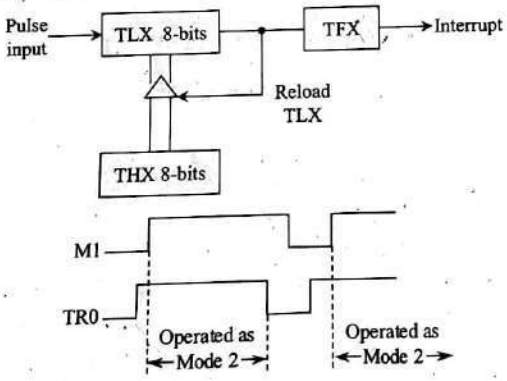


Figure (3)

$C/\overline{T} = 0 \rightarrow$ Timer

$= 1 \rightarrow$ Counter

Mode 2:

M1 = TR0 = logic 1

Mode 3

Timer 0 and 1 may be programmed to be in mode 0, 1 or 2 independently. This does not hold good for mode 3. Placing timer in mode 3 causes it to stop counting. The control bit *TR*1 and the timer 1 flag *TF*1 are then used by timer 0. Timer 0 in mode 3 becomes two completely separate 8-bit counters *TL*0 is controlled by the gate arrangement and sets timer flag *TF*0 whenever it overflows from FFh to 00h. TH0 receives the timer clock 1 under the control of *TR*1 only and sets the *TF* flag when it overflows.

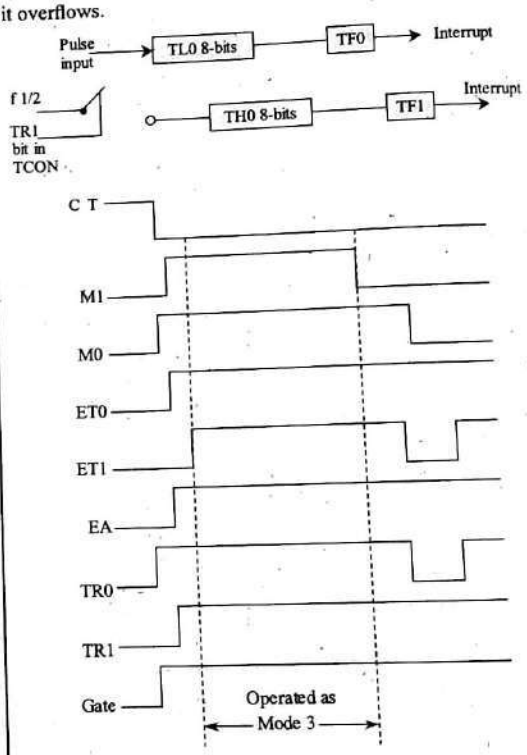


Figure (4)

$C/\overline{T} = 0 \rightarrow$ Timer

$= 1 \rightarrow$ counter

Mode 3:

M1 = M0 = ET0 = ET1 = EA = TR0 = TR1 = GATE = logic 1

5.5 SERIAL DATA INPUT/OUTPUT

Q22. Explain how serial data communication is done with 8051 serial ports.

(or)

Discuss in detail about serial port operation in 8051 microcontroller.

Serial Data Mode 2: Serial data mode 2 is also called as multi-processor mode. It is similar to mode 1 except 11-bits are transmitted, a start bit nine data bits and a stop bit, as shown in the figure (2).

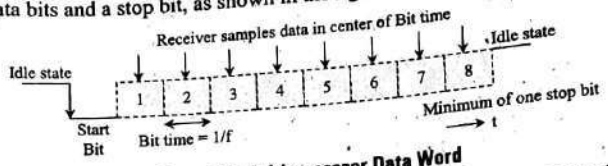


Figure (2): Multiprocessor Data Word

The 9th data bit is copied from bit *TB*8 in SCON during transmit and stored in bit *RB*8 of SCON when data is received. Both the start and stop bits are discarded.

The baud rate is programmed as follows,

$$f_{baud2} = \frac{2^{SMOD}}{64d} \times \text{Oscillator frequency}$$

The conditions for setting *R*1 for mode 2 are similar to mode 1. *R*1 must be 0 before the last bit is received and *SM*2 must be 0 or ninth data bit must be a 1 i.e.,

1. *R*1 = 0 and
2. Either *SM*2 = 0 or the received 9th data bit = 1

Serial Data Mode 3: Mode 3 is identical to mode 2 except that the baud rate is determined exactly as in mode 1, using timer 1 to generate communication frequencies.

5.6 INTERRUPTS

Q25. Discuss the interrupt structure of 8051. Mention the priority. Explain how least priority is made as highest priority.

Model Paper-III, Q6(a)

Ans:

Interrupt Structure of 8051: The 8051 have five interrupts which are available to users. But many manufacturers data sheets have six interrupts since they include Reset.

The six interrupts in 8051 are as follows,

1. Reset: when reset pin is activated the 8051 jumps to address location 0000.
2. Two from the timer/counter overflow flags, one for timer 0 and one for timer 1. Memory locations 000BH and 001BH in the interrupt vector table belong to timer 0 and timer 1 respectively.
3. Two interrupts from external inputs (INT0 and INT1). Pins of port 3, port 3-bit 2 (P3.2) and port3 - bit 3 (P3.3) are for external hardware interrupts INT0 and INT1 respectively. These external interrupts are also referred to as EX1 and EX2. Memory locations 0003H and 0013H in the interrupt vector table are assigned to INT0 and INT1.
4. One from serial port (*T*1 or *R*1) both for transfer and receive. Memory location 0023H in the vector table belongs to this interrupt. Table below shows the interrupt vector table for the 8051.

Interrupt	ROM Location (Hex)	Pin
Reset	0000	9
External hardware interrupt to (INT0)	0003	P3.2(12)
Timer0 interrupt (TF0)	000B	–
External hardware interrupt 1 (INT1)	0013	P3.3(13)
Timer 1 interrupt (TF1)	001B	–
Serial COM interrupt (Rl and Tl)	0023	–

Table: Interrupt Vector Table

Enabling and Disabling an Interrupt: Upon reset, all interrupts are disabled (masked), that is none of them will be recognized by the microcontroller, even if they are activated. The interrupts must be enabled by software, so that the microcontroller can respond (recognize) to them. A register called IE (Interrupt Enable) is used for enabling (unmasking) and disabling (masking) the interrupts.

Figure (1) shows IE register, it is bit addressable register.

7	6	5	4	3	2	1	0
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Figure (1): The Interrupt Enable (IE) Special Function Register

IE.7 EA : Enabled Interrupt Bits: Disables all interrupts, if *EA* = 0 and no interrupts will be recognized (acknowledged). If *EA* = 1, each interrupt source is individually enabled, or disabled by setting or clearing its enable bit.

IE.6 : Reserved

IE.5 ET2: Enabled Timer 2 Overflow Interrupt: If ET2 = 1 the timer 2 overflow or capture interrupt is enabled. If ET2 = 0, the timer 2 interrupt is disabled.

IE.4 ES: Enabled Serial Port Interrupt: ES = 1, enables serial port interrupt and ES = 0, disables serial port interrupt.

IE.3 ET1: Enabled Timer 1 Overflow Interrupt: ET1 =1, enables overflow interrupt and ET1 = 0, disables it.

IE.2 EX1 : Enabled External Interrupt 1: EX1 = 1, enables it and EX1 = 0 disables it.

IE.1 ET0: Enabled Timer 0 Overflow Interrupt: ET0= 1, enables it, ET0 = 0 disables it.

IE.0 EX0: Enabled External Interrupt 0: EX0 = 1, enables it, EX0 = 0 disables it.

Interrupt Priorities: Interrupt priority register (IP) determines, whether an interrupt has higher priority or lower priority. Figure (2) shows priority interrupt register.

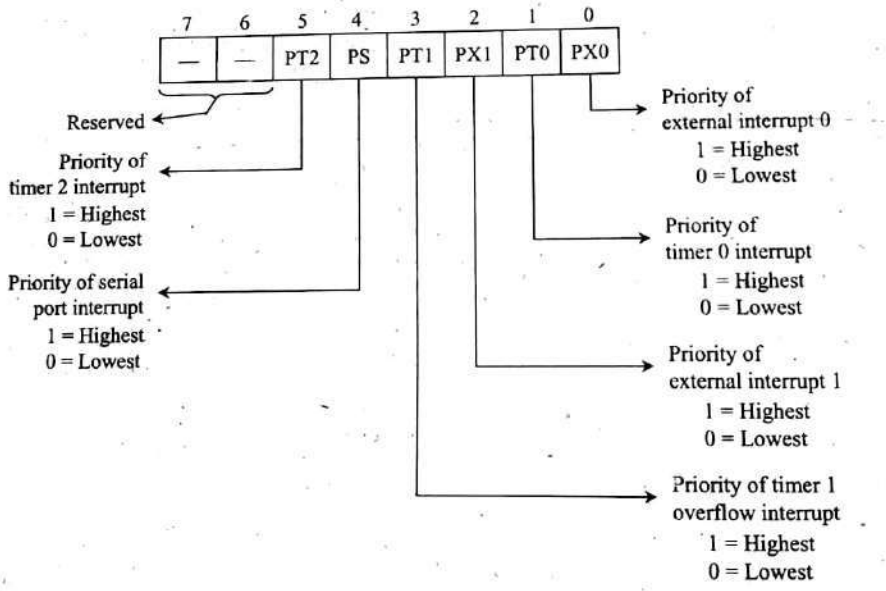


Figure (2): Interrupt Priority (IP) Special Function Register

Bits set to 1 indicates higher priority and bits cleared to 0 indicates lower priority. Interrupts with a high priority can interrupt another interrupt with a low priority, the lower priority interrupt continues after the higher is finished.

If two interrupts with the same priority occurs at a time, then the following priority level can be used.

Example

The serial interru

Q26. Give the sequ

Ans:

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Steps in Executing ar

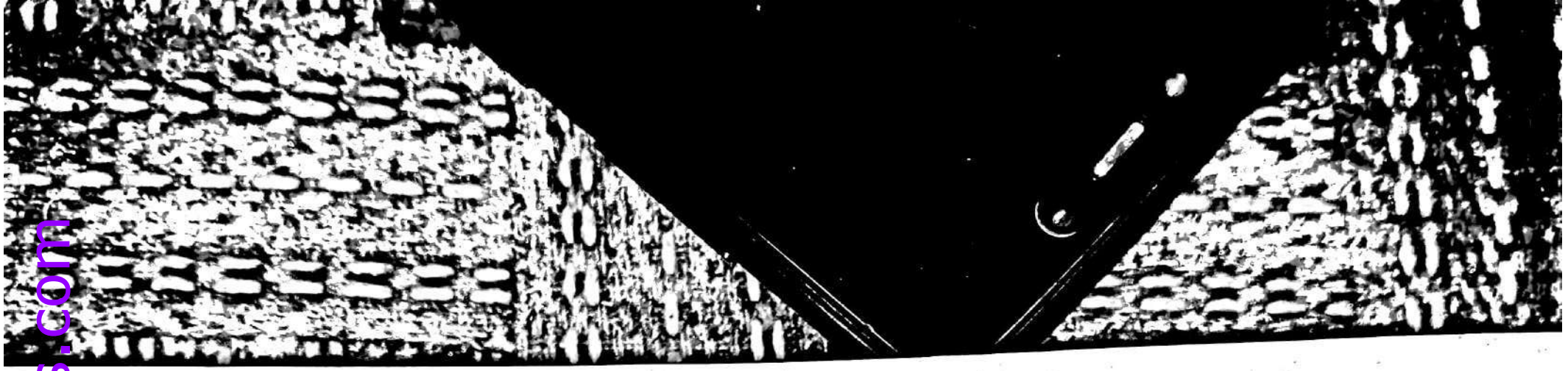
Once the interr

1. It finishes the i
2. It also saves th
3. It jumps to a fi
4. The microcon interrupt serv
5. Upon executi Program Cou execute from

Q27. Discuss or

Ans:

External Interrup



	Interrupt	Priority Level
1.	External Interrupt 0 (IE0)	Highest
2.	Timer/Counter 0 overflow (TF0)	-
3.	External Interrupt 1 (IE1)	-
4.	Timer/Counter 1 overflow (TF1)	-
5.	Serial (R1 or T1)	Lowest

ıl interrupt could be assigned the highest priority by setting PS bit in IP register to '1' all others

to that takes place when the interrupt occurs in 8051.

5.8 INTERFACING: KEYBOARD, DISPLAYS (LED, 7-SEGMENT DISPLAY UNIT), A/D AND D/A CONVERTERS

Q41. With a neat circuit diagram explain how a 4 × 4 keypad is interfaced with 8051 microcontroller and write 8051 ALP for keypad scanning.

Ans:

The interfacing of 4 × 4 matrix keyboard with 8051 is depicted in figure.

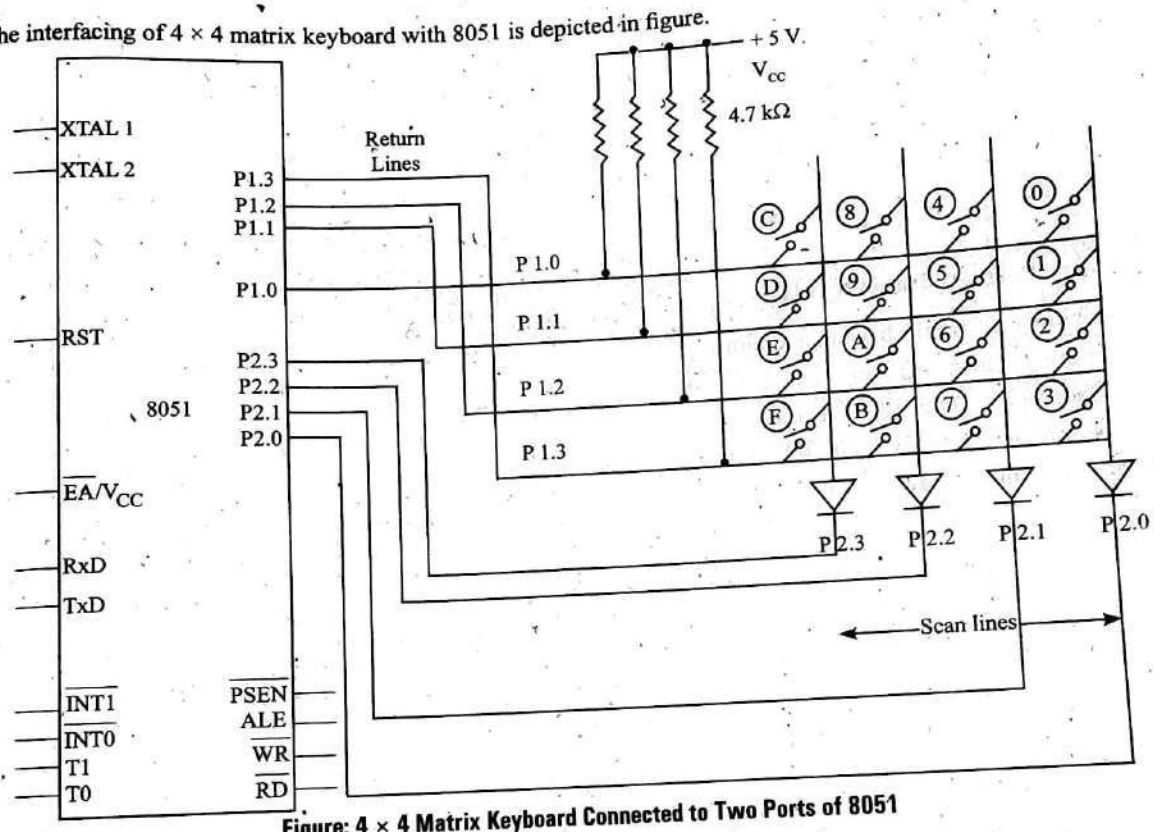


Figure: 4 × 4 Matrix Keyboard Connected to Two Ports of 8051

Keyboards are arranged in a form of matrix which contains rows and columns. These rows and columns are connected to ports. So, they are accessed by CPU using the ports. Thus, 4 × 4 matrix of keys is connected to microprocessor using two ports of 4-bits each. If no key is pressed then there won't be any contact (or) connection between the rows and columns. If any key has been pressed, there exist a connection between rows and columns.

The steps in algorithm are as follows,

1. Initialize pins of port 1 (P1.1, P1.2, P1.3) as output.
2. The pins of port 2 P2.0 - P2.3 are initialized with '0' to ensure all the keys are released. State '1' return lines indicates keys are not pressed.
3. Call debounce.
4. Wait for key pressing. All the scan lines yields '0' because they are grounded and check whether any one of the return line shows '0'. When the key is pressed it goes to next step. Otherwise, it resides in step 4 itself until the key is pressed.
5. Call debounce.
6. Check whether the key is really pressed or not. If 'No' go to step 4.
7. Find key code and display the key number which has been pressed on the 7- segment LCD.
8. Go to step 1.

Q42. Explain the interfacing of LED with 8051.

Ans:

Light Emitting Diodes (LEDs) are the electronic devices which are available in different sizes (3, 5 and 8 mm), shapes (circular, rectangular) and colors (Red, Yellow, Green, Blue, White and Orange). These are used as indicators to display ON and OFF states. Generally, Red LEDs of 5 mm size are used as general purpose indicators. The symbol for an LED is as shown in figure(1).

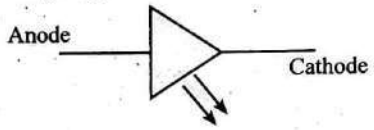


Figure (1): Symbol of an LED

LEDs glow on forward biasing and allow all the current to flow through them i.e., they offer zero resistance. In order to interface an LED with 8051, the limiting current of 15 mA should be supplied by the port pin, if the LED is of high-intensity, current limit should be 7 mA. Figure (2) illustrates the interfacing an LED with 8051 in logic 0 and logic 1 states.

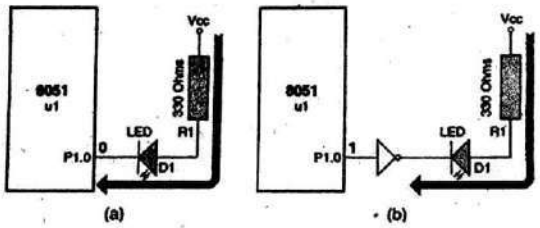


Figure (2)

From figure (2), the resistor connected in series to the LEDs current limiting resistor limits the current according to LED. Port pin (P1.0) of 8051 drives the LED in logic 0 or logic 1 state.

Case 1: In logic state 0, LED is directly connected to port pin, which provides enough current to turn ON LED.

Case 2: In logic state 1, the direct connection of LED to port pin results in insufficient limiting current such that LED doesnot turn ON. To avoid this, LED is connected to port pin via buffer which provides adequate current to turn ON the LED.

Q43. Explain the interfacing of seven segment display with 8051.

Ans:

Interfacing of 7-segment display with 8051 microcontroller is as shown in figure (1),

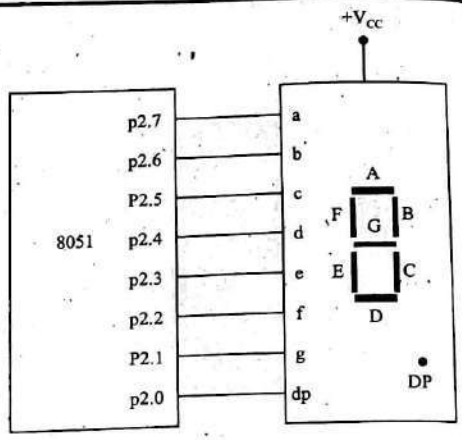


Figure (1): 8051 Connected to a 7-segment Display

From figure (1), it can be observed that, 7-segment display consists of an array of LED's arranged in a 2-D plane. When LED's are forward biased it emits light and displays numbers from (0-9) and (A-F). There are basically two types of displays,

1. Common – anode display
2. Common – cathode display.

In common-anode display, all the anodes connected together whereas, in common cathode display all the cathodes connected together as shown in figure (2),

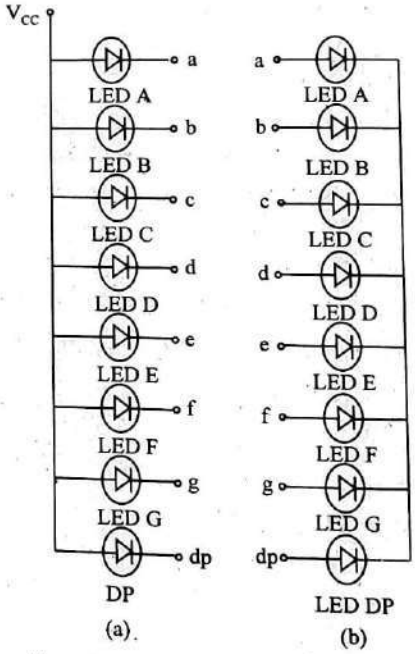


Figure (2): (a) Common Anode Connection

(b) Common Cathode Connection

The codes to display the numbers on the 7-segments display is shown in table below,

Number	Code	LED Status							
		A	B	C	D	E	F	G	DP
0	03	0	0	0	0	0	0	1	1
1	9F	1	0	0	1	1	1	1	1
2	25	0	0	1	0	0	1	0	1
3	0D	0	0	0	0	1	1	0	1
4	D9	1	1	0	1	1	0	0	1
5	49	0	1	0	0	1	0	0	1
6	41	0	1	0	0	0	0	0	1
7	1F	0	0	0	1	1	1	1	1
8	01	0	0	0	0	0	0	0	1
9	19	0	0	0	1	1	0	0	1

Table

Operation

To display any number in 7-segment display the corresponding input pins are made high and low to switched ON the LED's and switched OFF the LED's, respectively.

For example, to display the number zero in 7-segment common-anode type display. A low input is applied to the pins *a*, *b*, *c*, *d*, *e*, *f* and high input is applied to pins '*g*' and *dp*, due to this LED's *A*, *B*, *C*, *D*, *E*, *F* are switched ON and LED's *G* and *DP* are switched OFF. Thus, number zero is displayed. Similarly by applying different inputs with respect to its codes to the 7-segment display its corresponding number is displayed.

Q44. Explain the interfacing of 0809 ADC with 8051 and write the programming of ADC0809 in Assembly and C.

Ans: The interfacing of ADC0809 to 8051 is as shown in figure (1).

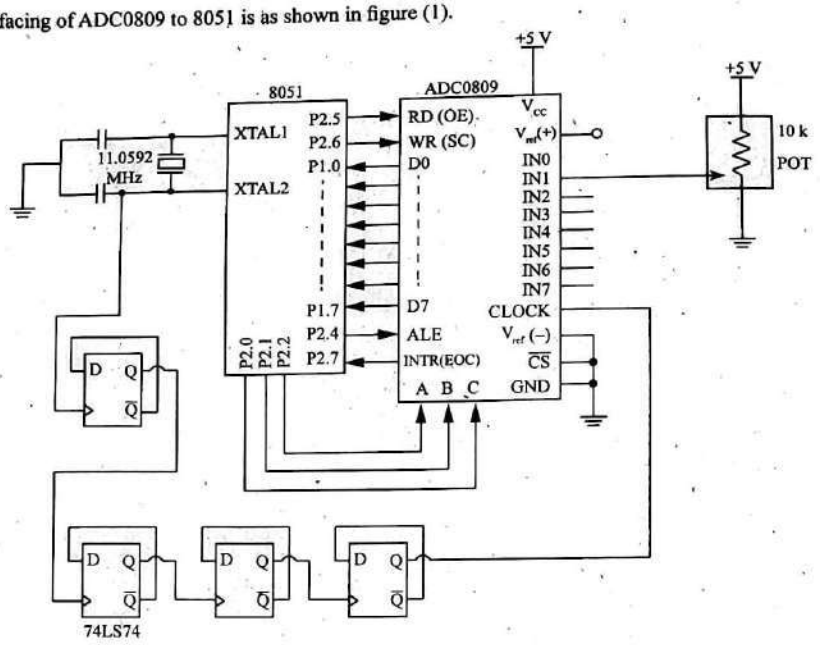


Figure (1)

The bits *A*, *B* and *C* selects the analog channels (IN0 .... IN7). A low-to-high pulse activates AL (Address latch enable). Similarly, the conversion is initiated by activating SC by an low to high pulse. The external clock connected to CLK pin produces a delay such that the converted digital data can be read easily.

After the end of conversion, EOC is activated by an high to low output. A low to high pulse on Output Enable (OE) is used to read data out of the ADC chip.

The channel selection and reading of data is illustrated in figure (2).

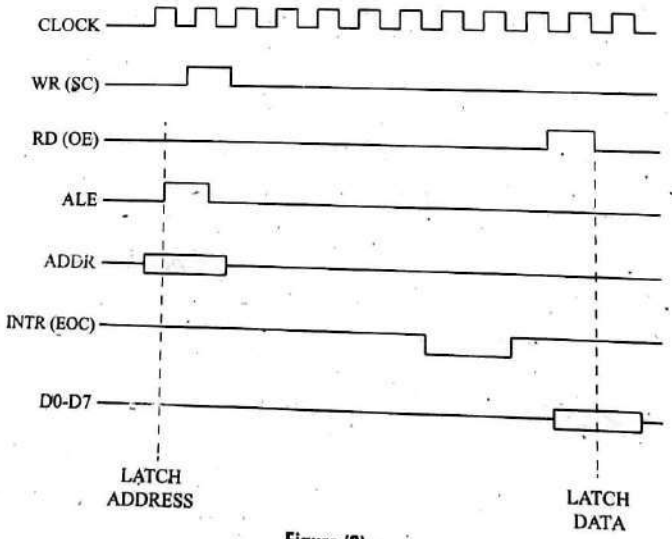


Figure (2)

Q45. Describe the basic operation of DAC chip with 8051.

Ans: The interfacing of DAC0808 with 8051 is as shown in figure below.

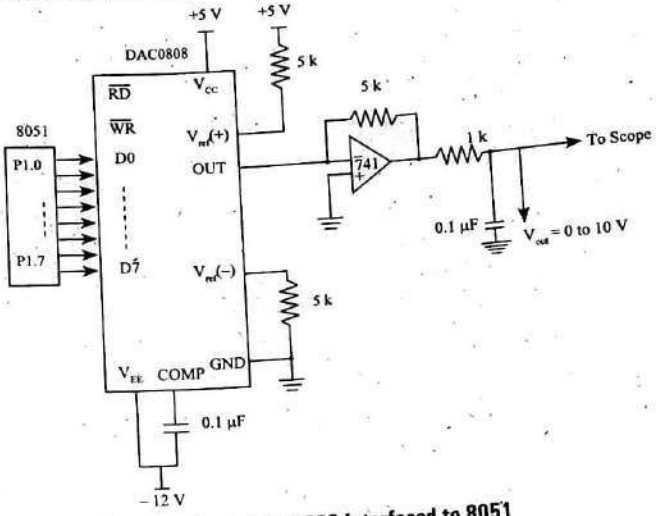


Figure: DAC0808 Interfaced to 8051

The port P1 of 8051 is interfaced with the digital inputs of DAC. The output of the DAC is current which is converted into voltage using an op-amp. This analog output current depends on I_{ref} flowing through V_{ref} and status of D0 - D7 bits.

Hence, the current voltage is obtained as,

$$I_{out} = I_{ref}\left(\frac{D7}{2} + \frac{D6}{4} + \frac{D5}{8} + \frac{D4}{16} + \frac{D3}{32} + \frac{D2}{64} + \frac{D1}{128} + \frac{D0}{256}\right)$$

Where,

D0 - LSB

D7 - MSB.

The analog output voltage is calculated as,

$V_{out} = I_{out} \times$ Feedback resistance