6. LOW POWER VLSI DESIGN [CMOS Logic circuits]

Introduction:- untill, recently performance has been synonymous with circuit speed or processing power. Eg: MIPS (multiple Instructions per second or MFLOPS (Mega flops).

→ power consumption were of secondary concern.

→ In Nanometer (Deep submicron) technology, power has become the most important issue because of

* Increasing transistor counts
* Higher speed of operation
* Greater device leakage currents.

Need for Low power:-

→ Increased process parameter variability due to aggressive scaling has created problems in yield, reliability and testing.

→ packing and cooling cost get increased if we have increased power dissipation and it should be prohibited.

→ So, low-power methodology to be used to reduce cost of packaging and cooling.

→ Increasing power density of VLSI chips: As devices are becoming smaller and smaller power density was increasing more and more as almost like Hot plate (pentium processor). so, we need to limit power density.

→ Increased customer demand for hand-held battery operated devices such as cell-phones, PDA, palamlop, laplop etc.

Cellphones with limitless functionality and limitless supply is the requirement.

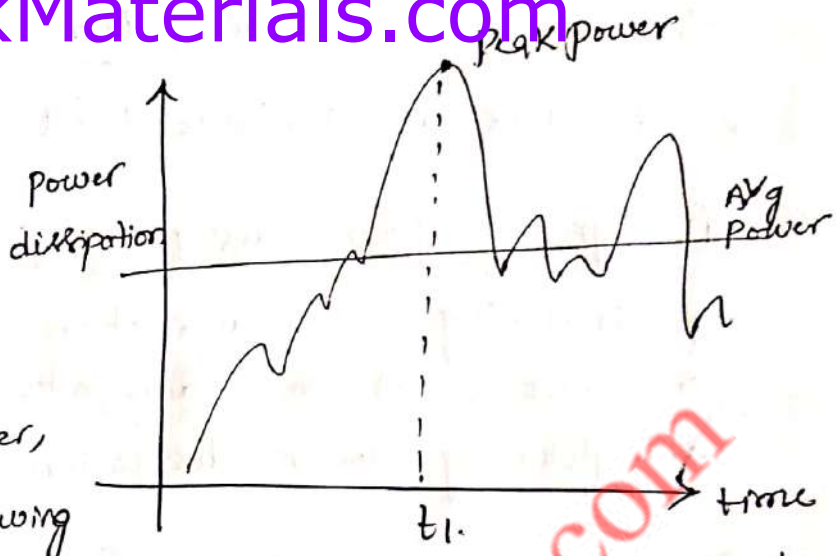
As these devices are battery operated, battery life is of primary concern. unfortunately, the battery technology has not kept up with energy requirement of portable equipme

so low power design is required to make these commercial viable.

→ Reliability:- very important in VLSI design. For every 10° rise in temperature roughly doubles the failure rate. So, to make the chip reliable, it is very important to use low-powe VLSI design methodology

Conclusion:- Considering the above all statements, a low-power design is very much important.

Power vs Energy:-



Peak power:- It is the maximum instantaneous power at particular time.

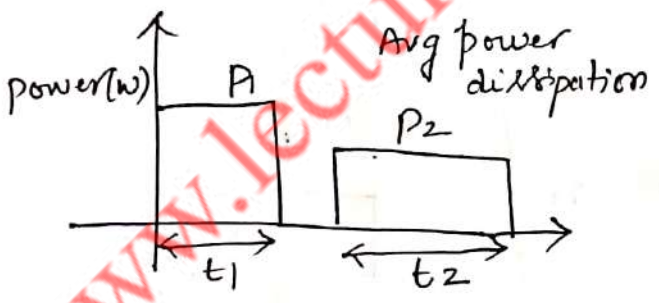
→ When we have peak power, some heavy currents are flowing through the chip line of finite resistance, so. voltage drop is there in power line & so called as glitches.

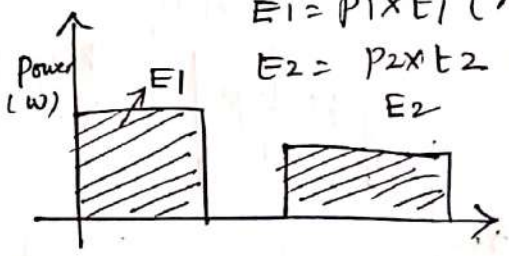
→ Glitches may lead to malfunction of chip & effects reliability of chip

Avg power:- Avg power effects the packing & cooling systems

Energy:- Rate at which energy is drawn from power source is the power dissipation.

Energy effects → Battery life.

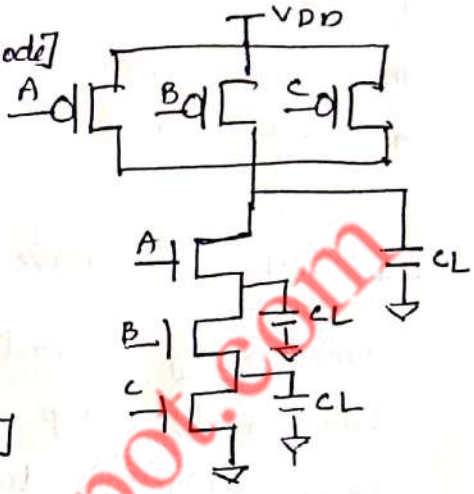




Note:- E1 & E2 are same but avg power is different.

→ In low power design, Energy is most important one. when we say low power, essentially low energy.

Sources of power dissipation: Junction capacitance may arised, those are parasitic load capacitances from below fig.



(i) **Dynamic power dissipation.** [ckt Active mode]

→ switching power dissipation
→ short circuit power dissipation
→ Glitching power dissipation.

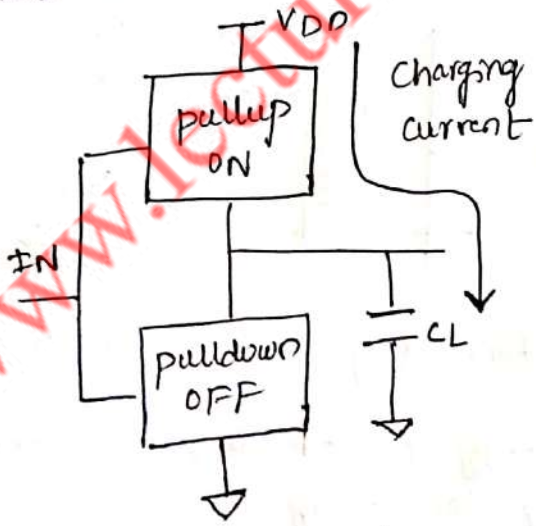
(ii) **Static power dissipation** [ckt Inactive/ Stand by mode]

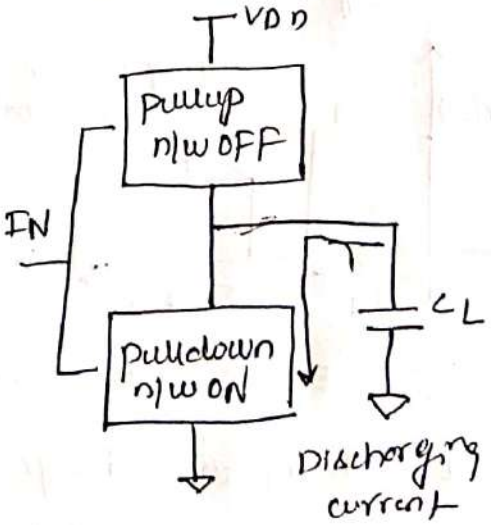
Due to

→ Diode leakage current
→ subthreshold leakage current
→ Gate leakage current.

Switching power dissipation: The power dissipation due to switching action. is called switching power dissipation

→ It is due to charging and discharging of parasitic capacitances.





→ Dynamic power dissipation (switching) is quite predominant in cmos design style.

→ Dynamic power is required to charge and discharge load capacitance when transistor switches.

→ one cycles involves arising & falling o/p's.

→ on rising ~~edge~~ o/p, charge $Q = CV_{DD}$ is required to charge the output node to V_{DD}.

→ on falling o/p, the load capacitor discharges to GND.

→ This repeats T x fsw times over an interval of T as shown below

where fsw – switching frequency

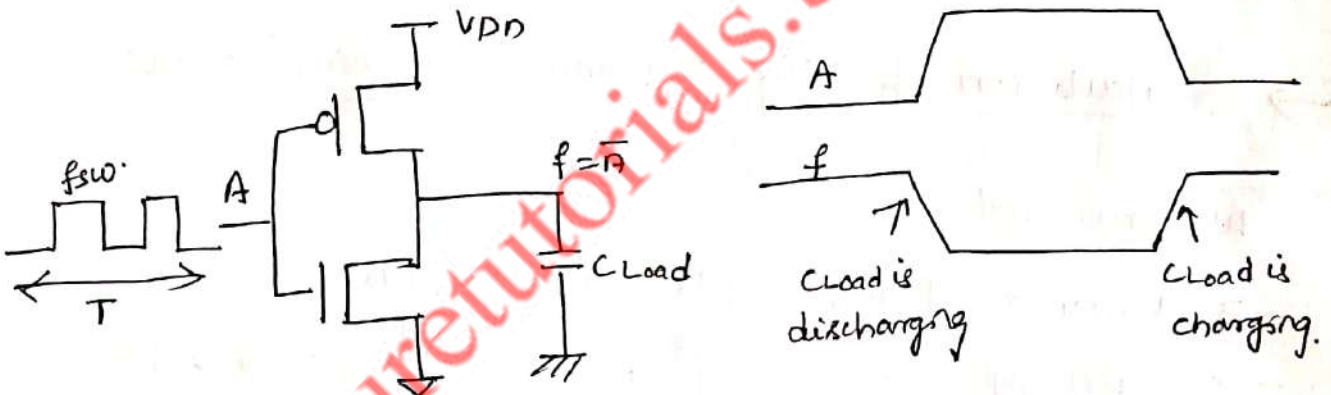


Fig:- Conventional cmos switching.

→ In complex logic gates, most of internal circuit nodes also make full or partial transitions during switching.

→ Since there is a parasitic capacitance associated with each internal node, these internal transitions contribute to the overall power dissipation of the circuit.

→ For example, let us consider a 2 i/p NOR gate that results in dynamic power dissipation as shown below

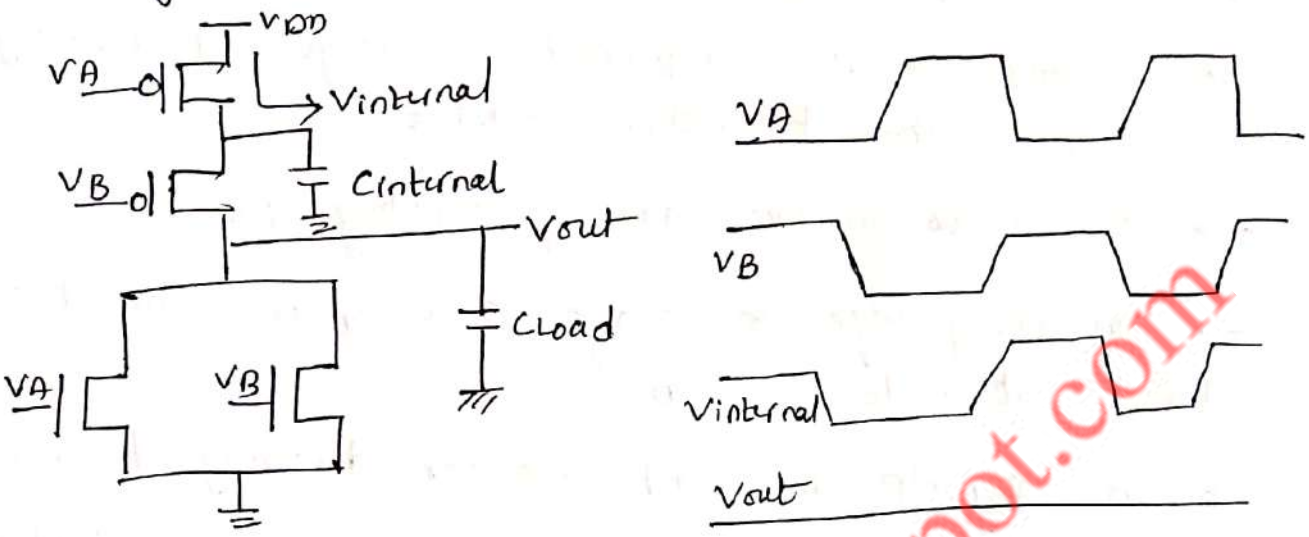


Fig:- switching of internal node in a 2 i/p NOR gate result in dynamic power dissipation even if o/p node voltage remains unchanged.

→ Calculation of avg dynamic switching power:-

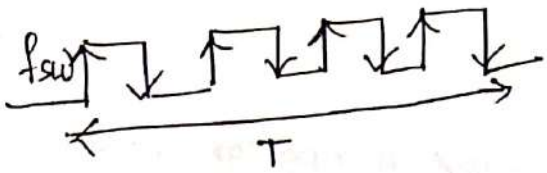
We know that-

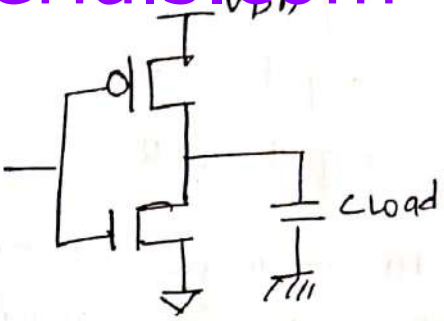
→ Instaneous power = $p(t) = i_{DD}(t) \cdot V_{DD}$.

→ Energy → $E = \int_0^T p(t)\,dt = \int_0^T i_{DD}(t) V_{DD}\,dt$

→ Avg power ⇒ $P_{avg} = \frac{E}{T} \Rightarrow \frac{1}{T}\int_0^T i_{DD}(t) V_{DD}\,dt$.

To calculate avg dynamic switching power dissipation, let us consider a CMOS with a switching frequency of 'fsw' over a time interval (0-T) as shown below





T x fsw = No. of switchings.

wkT

$V = \frac{1}{C}\int i(t)\,dt$

$dv_C = i(t)\,dt$

$C\,dV = i_{DD}(t)\,dt$

$P_{dynamic} = P_{avg}$

$P_{avg} = \frac{1}{T}\int_0^T i_{DD}(t) V_{DD}\,dt$

$\Rightarrow \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$

$\Rightarrow \frac{V_{DD}}{T}\int_0^T C\,dV\,dt$

$V \rightarrow V_{DD}$.

$dV \rightarrow V_{DD}$

$\Rightarrow \frac{V_{DD}}{T} C\,dV.(f_{sw} \times T)$.

$\Rightarrow \frac{V_{DD}}{T}(C V_{DD}) f_{sw} \times T$

$\therefore \int_0^T = f_{sw} \times T$

0 to T, multiple charges & discharges.

$C \rightarrow C_{load}$

$P_{avg} \Rightarrow C_{load} V_{DD}^2 f_{sw}$

Observations on switching Power reduction:-

We know that

$P_{avg} = C_{load} V_{DD}^2 f_{sw}$.

Pavg ∝ Cload

Pavg ∝ V_{DD}^2

Pavg ∝ fsw.

→ To minimize switching power dissipation, we have to reduce VDD, fsw, Cload.

→ If we minimize fsw (switching freq) the power dissipation is minimized but speed of operation is poor.

→ If we reduce supply voltage VDD, to minimize power dissipation. it is most widely preferable method for Low power design technique.

Activity factor:— A measure of how frequently o/p switching takes place

$$\therefore \boxed{f_{sw} = \alpha \cdot f_{clk}}$$ where

α – activity factor

f – clock frequency.

→ If the gate o/p directly drives the clock, ie; $\alpha = 1$

→ If gate o/p switches once per cycle, $\alpha = 1/2$.

Taking into account the activity factor α, the dynamic power of gate can be given as.

$P_{avg} = C_{load} V_{DD}^2 f_{sw}$. $\quad \because f_{sw} = \alpha f_{clk}$

$$\boxed{P_{avg} = C_{load} V_{DD}^2 \alpha f_{clk}}$$

Short circuit power dissipation:-

Let, a cmos inverter is driven with a input voltage of finite rise and fall times, both nmos & pmos transistors in the circuit may conduct simultaneously for a short amount of time during switching, which forms a direct path between the power supply and ground as shown below

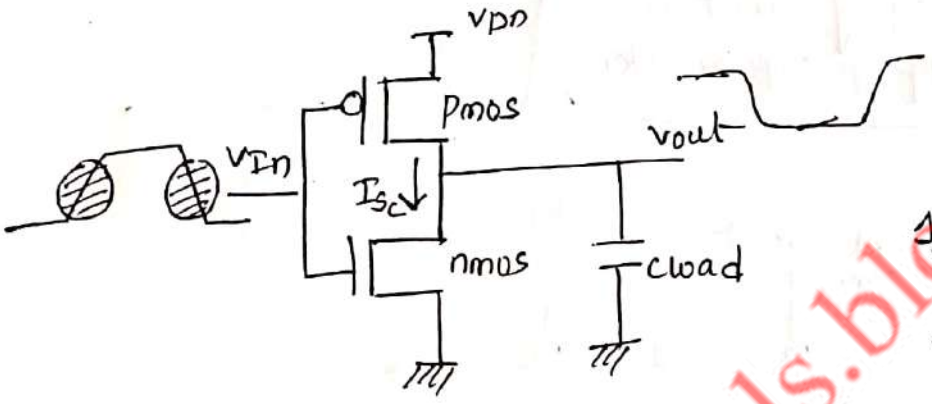


fig:- Both nmos & pmos may conduct simultaneously results in short circuit current Isc.

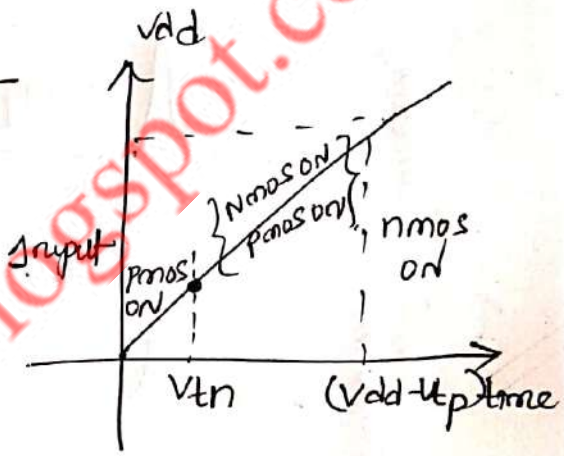
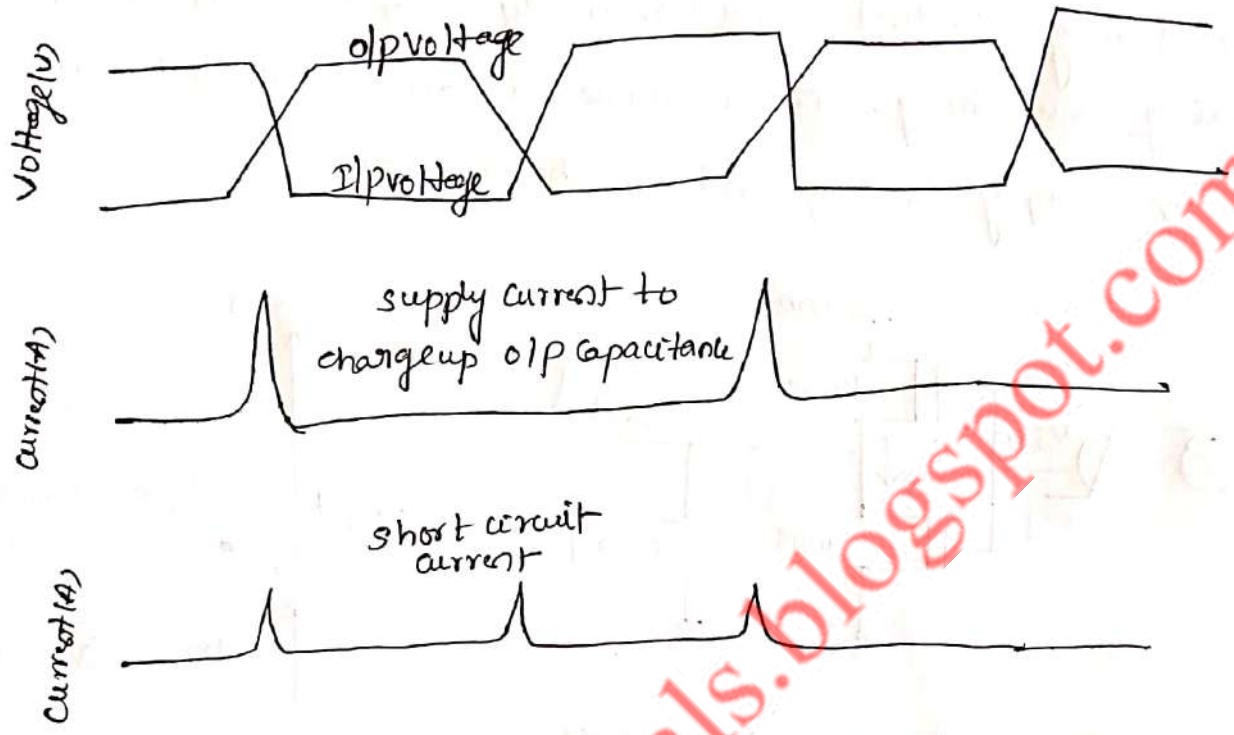


fig:- Graph that shows both pmos & nmos on regions

Note:- short circuit current is also called as crowbar current

→ As input changes slowly, power dissipation takes place when there is no load or parasitic capacitor. This is known as short circuit current

For a symmetrical CMOS inverter with small capacitive load, i/p & o/p voltage waveforms and components of current drawn from power supply are illustrated below



→ For a symmetrical cmos inverter, $K_n = K_p = K$.

$V_{T,n} = |V_{T,p}| = V_T$

$T_{rise} = T_{fall} = T$. Then the

avg short circuit current can be given as

$$I_{avg}(short\text{-}ckt) = \frac{1}{12}\frac{K T f_{clk}}{V_{DD}}(V_{DD} - 2V_T)^3$$

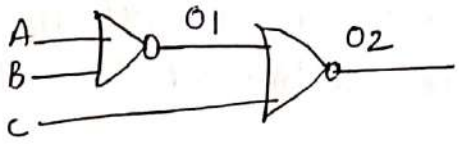
$$P_{avg}(short\text{-}ckt) \Rightarrow \frac{1}{12} K T f_{clk} (V_{DD} - 2V_T)^3$$

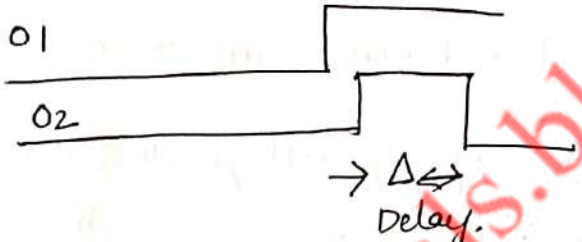
Note:— Short circuit power dissipation is linear proportional to rise & fall times, so reducing signal transition times will decrease the short circuit current component.

Glitch power dissipation:- When some heavy currents are flowing through the chiplines having finite resistance, some voltage may drop in power lines, called as glitches and the power dissipation due to glitches are named as glitch power dissipation.

→ Glitches are generated at o/p because of delay.

Eg:-





→ o/p waveform showing glitch at output O2.

Static power dissipation:- Static power is something which occurs even when there is no signal transitions.

→ static power is consumed even when the chip is quiescent

→ Leakage effects draw power from nominally OFF devices

→ Static power dissipation is due to

* Diode leakage current
* Subthreshold leakage current.
* Gate leakage current.

Leakage power dissipation:—

→ The nmos & pmos transistors used in cmos logic gate generally have non-zero reverse leakage & subthreshold currents.

→ In cmos VLSI chip containing very large number of transistors, these currents can contribute overall power dissipation when the transistors are not undergoing any switching event.

(i) → **Reverse diode leakage current:—** It is one of the main leakage current that occurs when pn-junction blw drain & bulk of the transistor is reverse biased.

→ The reverse-biased drain junction then conducts a reverse saturation current which is drawn from power supply.

→ For a cmos with high i/p voltage, the nmos 'on' and o/p node discharged to '0'. Although pmos off, there will be a reverse potential difference of VDD blw drain & n-well, causing a diode leakage through drain junction.

→ The n-well region of pmos transistor is also reverse biased with VDD, with respect to p-type substrate as shown below

→ when input voltage is 0, o/p charged to VDD through pmos. then reverse potential difference blw nmos drain & p-substrate causes reverse leakage current.

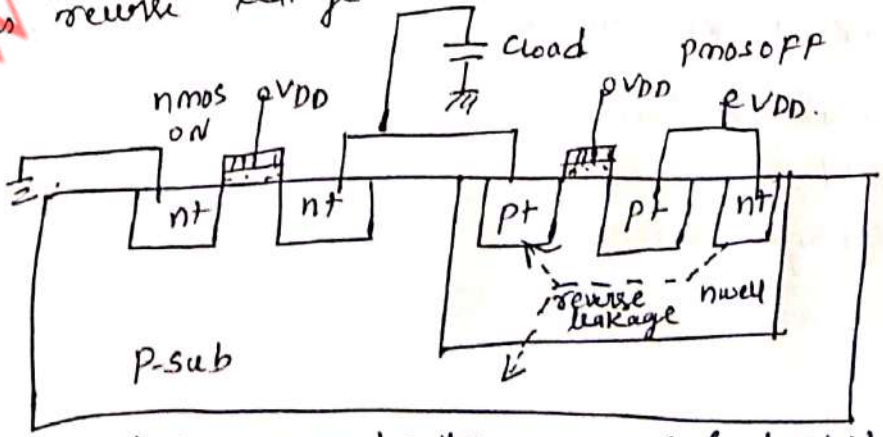


Fig:- Reverse leakage current paths in a cmos for high i/p voltage

The reverse leakage current of pn-junction is expressed by

$$I_{rev} = I_0\left(e^{\frac{qV_{bias}}{KT}} - 1\right)$$

$$J = \frac{I}{A}$$

$$I_{rev} \Rightarrow A \cdot J_s\left[e^{\frac{qV_{bias}}{KT}} - 1\right]$$

(i) Subthreshold leakage current:-

→ It is due to carrier diffusion between source and drain regions of the transistor in weak inversion.

→ Subthreshold leakage current can occur even when there is no switching activity in the circuit and this component can be considered for estimating the total power dissipation in stand by mode.

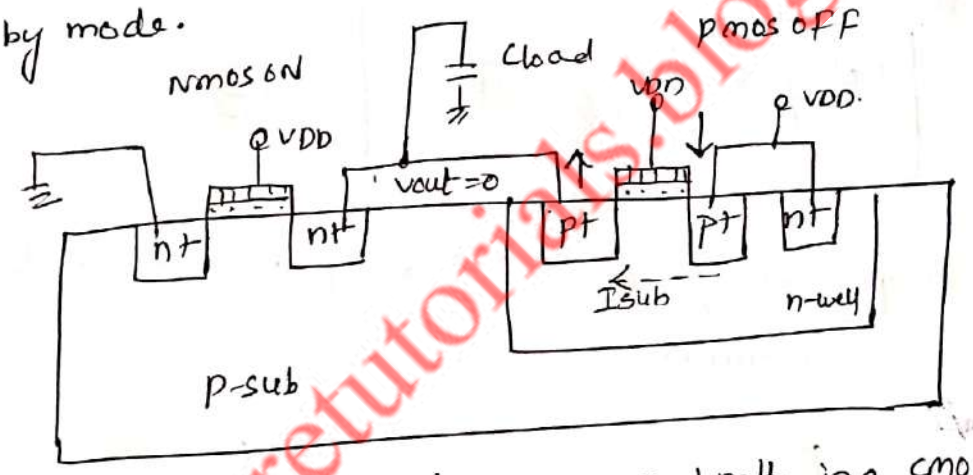
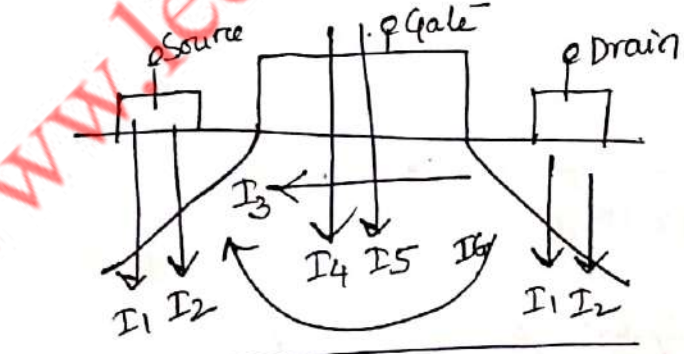


fig:- Subthreshold leakage current path in a cmos inverter with high input voltage.



I_1 - Reverse bias pn-junction diode leakage current

I_2 = Band-to-Band tunneling leakage current

I_3 = subthreshold leakage current

I_4 = Gate oxide tunneling current

I_5 = Gate current due to hot carrier injection

I_6 = Channel punchthrough current

Low power design through voltage scaling :-

$$P_{avg} = C_{load} V_{DD}^2 f_{sw} \quad \text{—(1)}$$

→ Challenges in supply voltage scaling :-

→ A factor of two reduction in supply voltage yields a factor of four decrease in Energy

→ Theoritical lower limit of supply voltage for cmos is 0.2V.

→ The relation b/w supply voltage, threshold voltage & delay may be given as

$$\text{Delay} \propto \frac{1}{V_{DD}\left(1-\frac{V_t}{V_{DD}}\right)^2} \quad \text{—(2)}$$

→ As supply voltage is lowered, delay increases leading to dramatic reduction in performance.

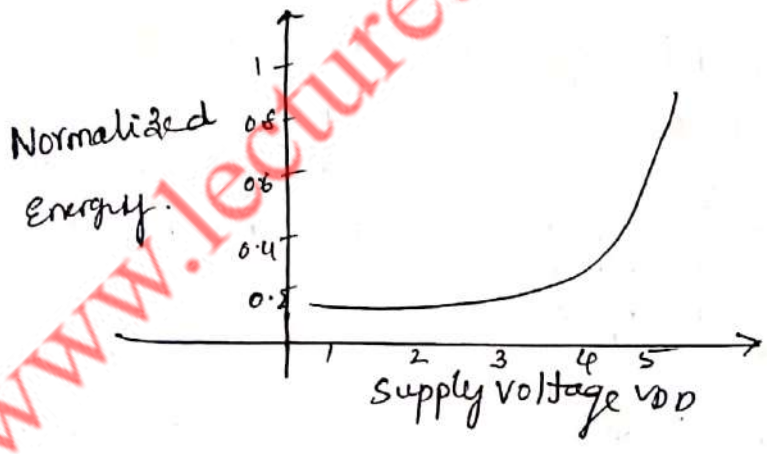


Fig: Energy vs supply voltage

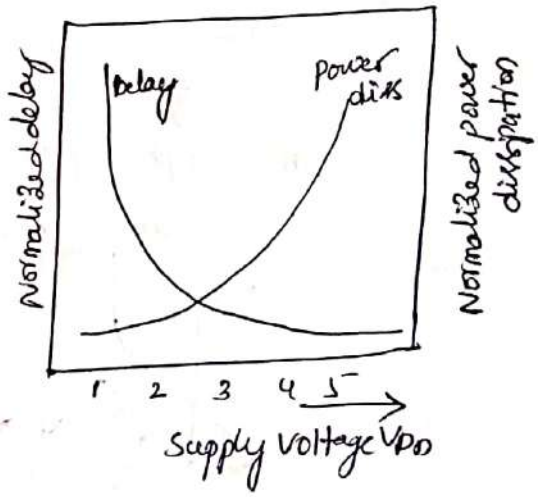


Fig:- Delay, Power dissipation vs. VDD

→ From eqn (2), V_{DD} is equal to about V_{DD} - V_t then $\left(1 - \frac{V_t}{V_{DD}}\right)^2$ is very small, then delay is high. which is a serious problem.

→ So, Instead of decreasing V_{DD}, decrease V_t, to minimize delay.

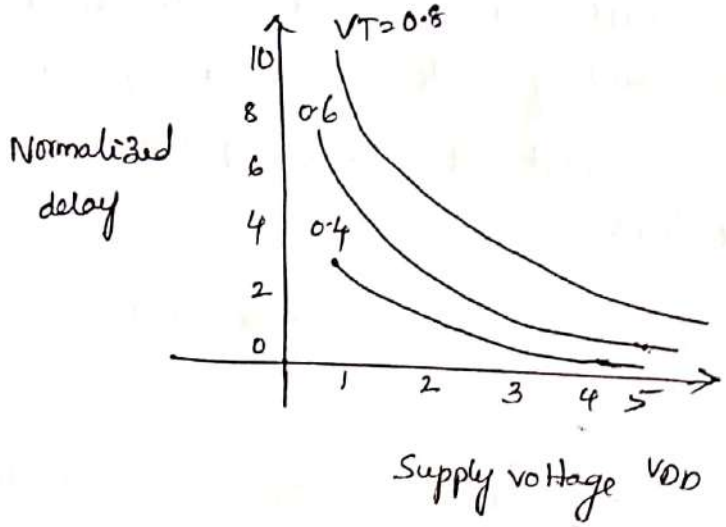


Fig:- Delay vs V_{DD} at different V_t values.

Note:-

→ Decreasing the value of threshold voltage (V_t), may result in a weak inversion layer, which allow a leakage current b/w Drain to Source.

ie; subthreshold current arised if V_t is decreased in stand by mode which may cause power dissipation.

Prediction:- To overcome low 'Vt' problems (leakage current & high standby power dissipation), we will use low 'Vt' design technique to supplement above problems. They are.

1) VTCMOS (variable threshold cmos)
2) MTCMOS (Multi threshold cmos)

(1) Variable threshold CMOS (VTCMOS) circuit:-

→ Low V_{DD} and low 'Vt' in a cmos circuit, is an efficient method for reducing overall power dissipation, while maintaining high speed performance.

→ But low 'Vt' may result in increased subthreshold leakage current which cause high stand by mode power dissipation.

→ TO overcome this, we adjust 'Vt' to avoid leakage in stand-by mode. by changing substrate bias.

→ The threshold voltage 'Vt'. of a mos transistor is a function of source to substrate bias V_{SB}.

→ In conential cmos, pmos substrates are connected to VDD & NMOS substrate terminals are connected to GND respectively.

→ This ensures that source & drain diffusion regions are always remain reverse biased with respect to substrate and does not influenced by body (back gate) bias) effect.

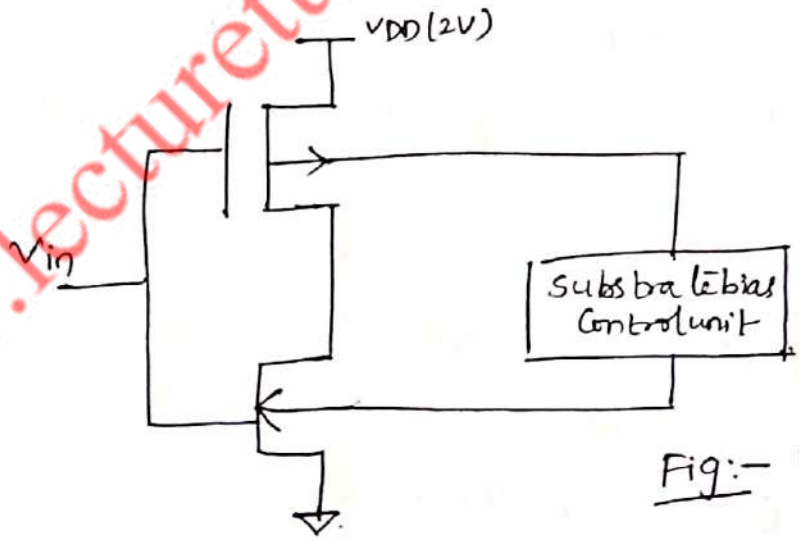


Fig:- VTCMOS inverter

Active mode:- Low threshold voltages.

V_{BP} = 2V(VDD), V_{tp} = −0.2V, V_{BN} = 0V, V_{tn} = 0.2V

Stand by mode:-

V_{BP} = 4V, V_{tp} = −0.6V, V_{BN} = −2V, V_{tn} = 0.6V.

Operation of VTCMOS:-

Active mode:- Substrate bias of nmos is $V_{Bn}=0$ and substrate bias voltage of pmos is $V_{BP}=V_{DD}$. Thus inverter transistors donot experience any backgate bias effect.

The circuit operates with low V_{DD} & low V_T, benefiting low power dissipation & high switching speed.

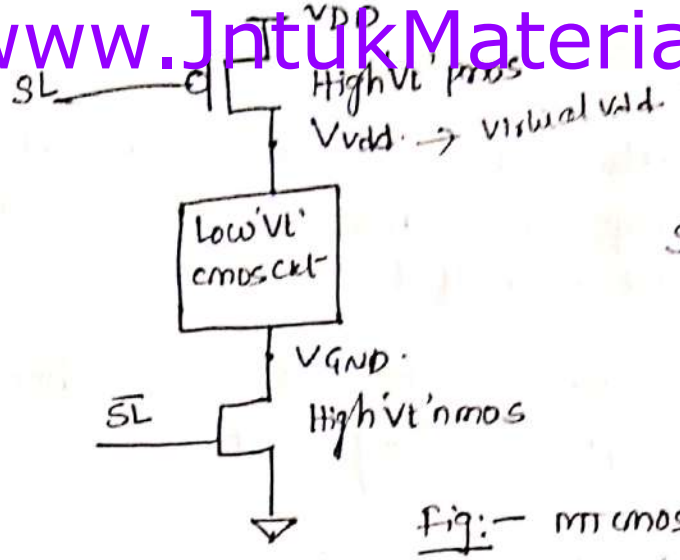
Standby mode:- In this, substrate bias control unit generates lower substrate bias voltage for nmos & higher substrate bias voltage for pmos transistor.

As a result, V_{tn}, V_{tp} both increase, due to backgate bias effect. Since subthreshold leakage current drops exponentially with increase in threshold voltage. Hence minimum power dissipation.

VTCMOS can also be used to control 'Vt' automatically to reduce leakage currents and this approach is called self-Adjusting Threshold-voltage scheme (SATS).

Multiple-Threshold CMOS (MTCMOS) circuits:- MTCMOS is a technique that uses two different voltages in the circuit inorder to reduce leakage currents.

The generic circuit structure of the MTCMOS logic gate is shown below

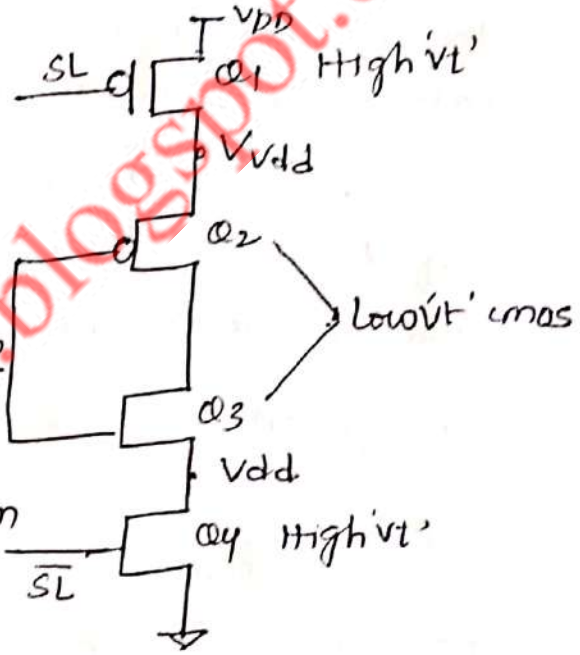


SL & $\overline{SL}$ are sleep control signals.

Fig:- MTCMOS ckt

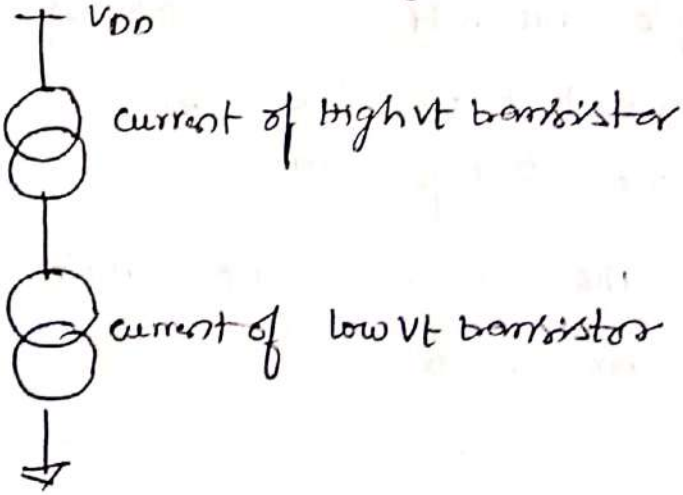
MTCMOS can be operated in two modes.

* Normal mode:- Here Q1 & Q2 are ON and these are high Vt cmos circuits. So current passing through the circuit is dependent on Q2 & Q3.



→ When Vin is '0' V, then Q3-OFF, so leakage current will be a dependent on leakage current of Q3 transistor.

* In Active mode:- Make Q1 & Q2 OFF, then Vvdd & VGND are no longer virtual VDD and no longer virtual GND.



When two currents are in series, lower current will flow through higher Vt circuits.

Advantages & Limitations of MTCMOS circuits:-

→ MTCMOS can be easily implemented using existing circuit.

→ MTCMOS reduces only the standby power.

→ Large inserted MOSFETs will increase area & delay

→ Extra Vth memory circuit is needed to maintain the data in the stand by mode.

Architecture level approaches for Static voltage scaling

1) Parallelism approach (Hardware replication)

→ Parallel processing can be an important technique for reducing power consumption in CMOS circuits.

→ The key approach is to trade area per power while maintaing the same throughput.

→ In simple terms, if the supply voltage is reduced by half the power is reduced by one-fourth and performance is lowered by half.

→ The loss in the performance can be compensated by parallel processing.

Eg:- Two 16-bit registers supplies two operands to a Adder as shown below

The estimated dynamic power of the circuit can be given as

$$P_{ref} = C_{ref} V_{ref}^2 f_{ref}$$

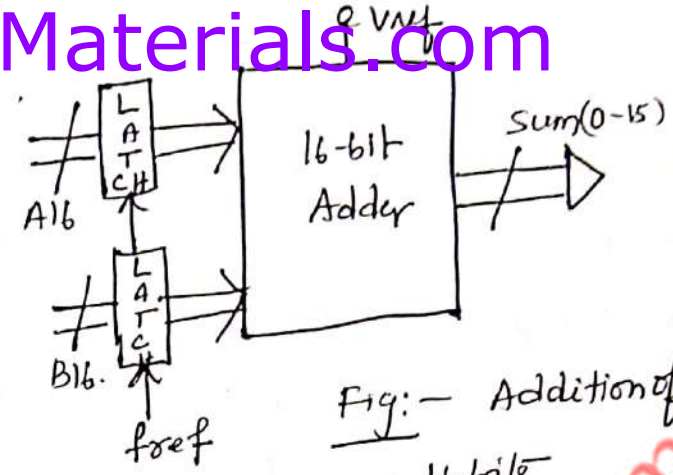
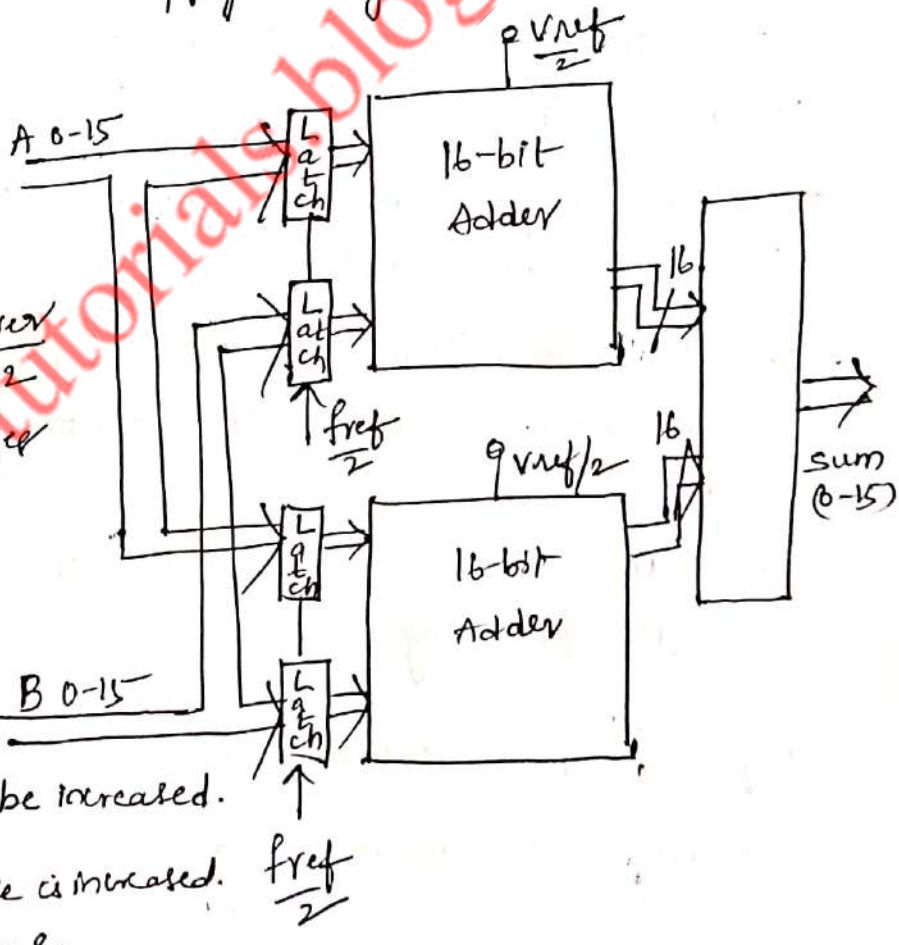


Fig:- Addition of two 16 bits

→ For parallelism, the adder has been duplicated twice, but the input registers have been clocked at half the frequency of fref.

→ This helps to reduce the supply voltage as shown below



wkt

$$P_{ref} = C_{ref} V_{ref}^2 f_{req}$$

$$P_{parallel} = 2.2 C_{ref} \left(\frac{V_{ref}}{2}\right)^2 \frac{f_{req}}{2}$$

$$\Rightarrow \frac{2.2}{8} C_{ref} V_{ref}^2 f_{req}$$

$$P_{parallel} = 0.227\, P_{ref}$$

ie, using parallelism the power is reduced thereby throughput can be increased.

Note:- For parallel capacitance is increased. ie, 2 times, theoritically 2.2 times.

The above example can be extended for 'N' no of logic functions as.

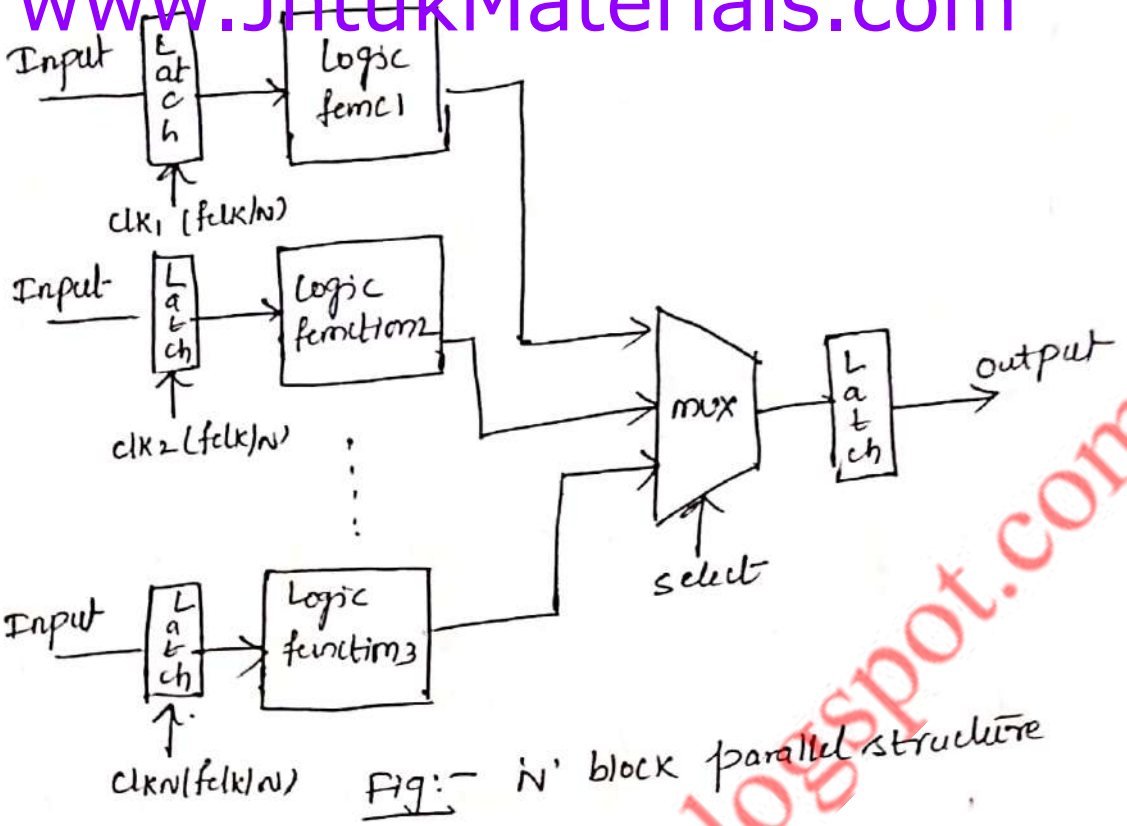


Fig:- N' block parallel structure

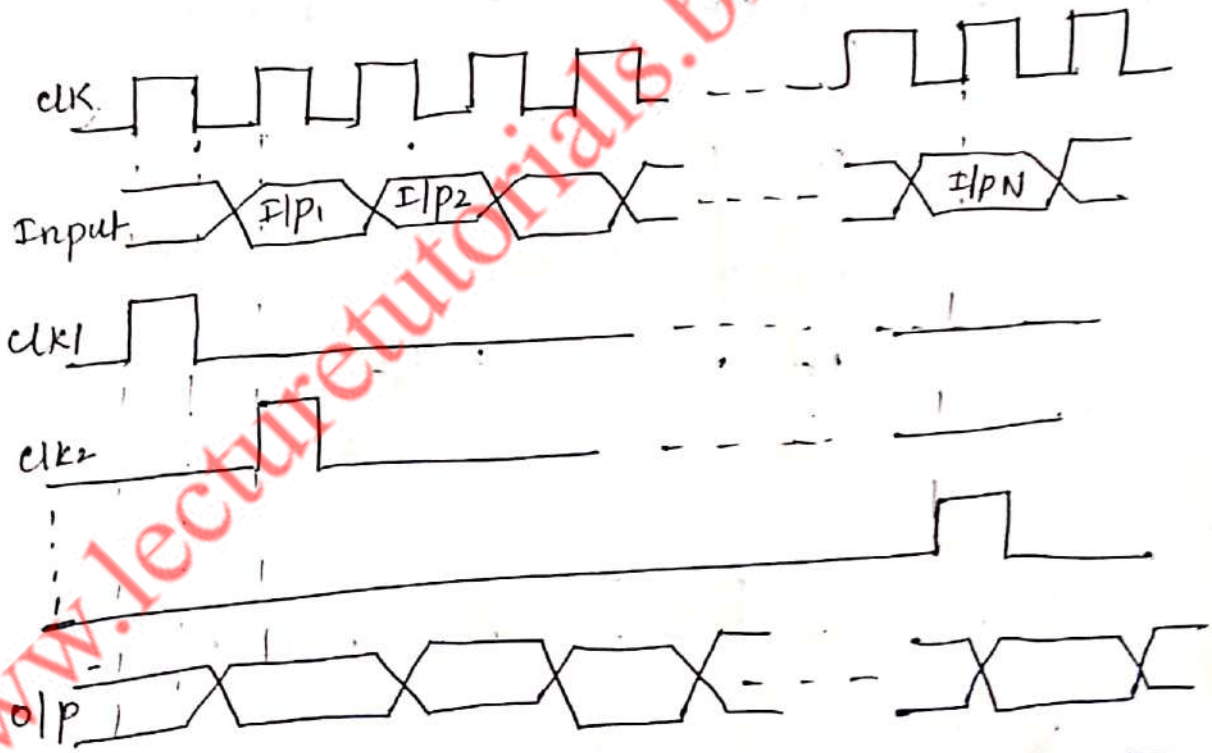


Fig:-Timing diagram for N-block parallel structure

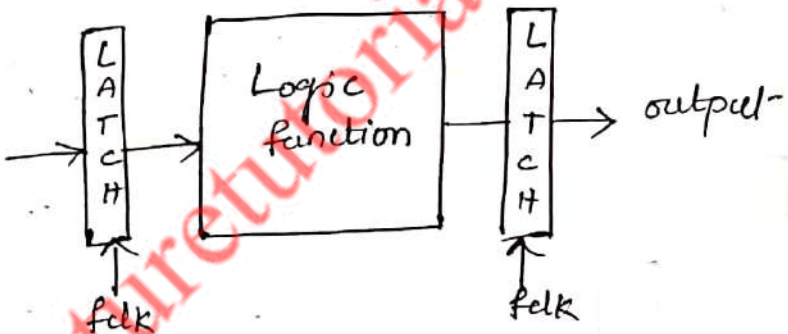
→ For 'N' no. of stages are considered if N↑ then power is more decreased.

→ For 'N' identical processing blocks, the freq is $\frac{f_{ref}}{N}$.

ie; The speed may be decreased by a factor 'N' which result in greater delay.

(2) pipelining approach:- pipelining approach is used to overcome the drawback of parallelprocessing ie, Delay can be reduced using pipelining approach.

It is an implementation technique where multiple tasks are performed in an overlaped manner.



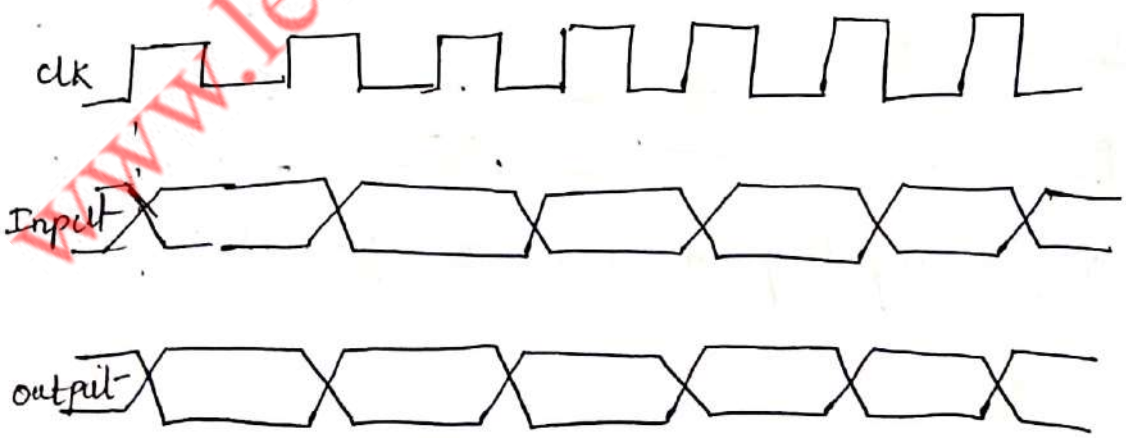


Fig:- Single stage implementation of a logic function & timing diagram.

Eg:- Instead of 16-bit addition, 8 bit addition is performed in each stage as shown below

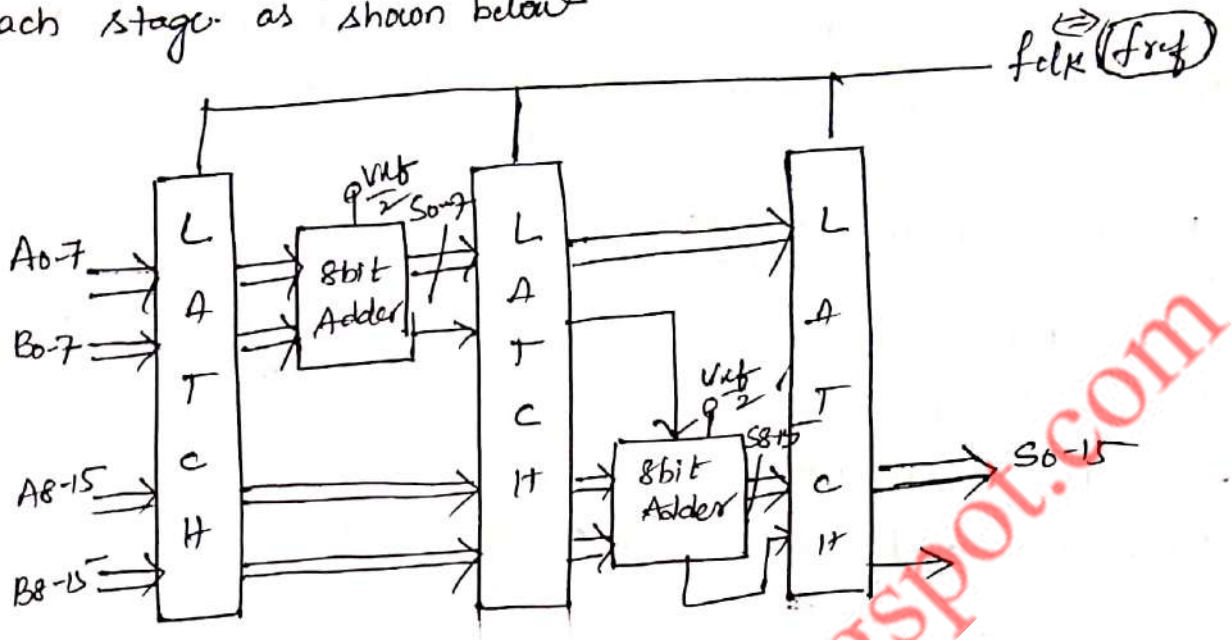


Fig:- 2-stage pipeling

→ In above circuit, 8bit adder will operate at a clock freq fref with a reduced power supply of $\frac{V_{ref}}{2}$.

→ We know that $P_{ref} = C_{ref} V_{ref}^2 f_{ref}$

$$P_{pipe} = (1.15 C_{ref}) \left(\frac{V_{ref}}{2}\right)^2 . f_{ref}$$

$$\boxed{P_{pipe} \approx 0.28 . P_{ref}}$$

Note:- In parallel processing, we have 2 parallel stages, so capacitance is increased to 2.2, but here no parallel stages. So capacitance is low. ie; 1.15.

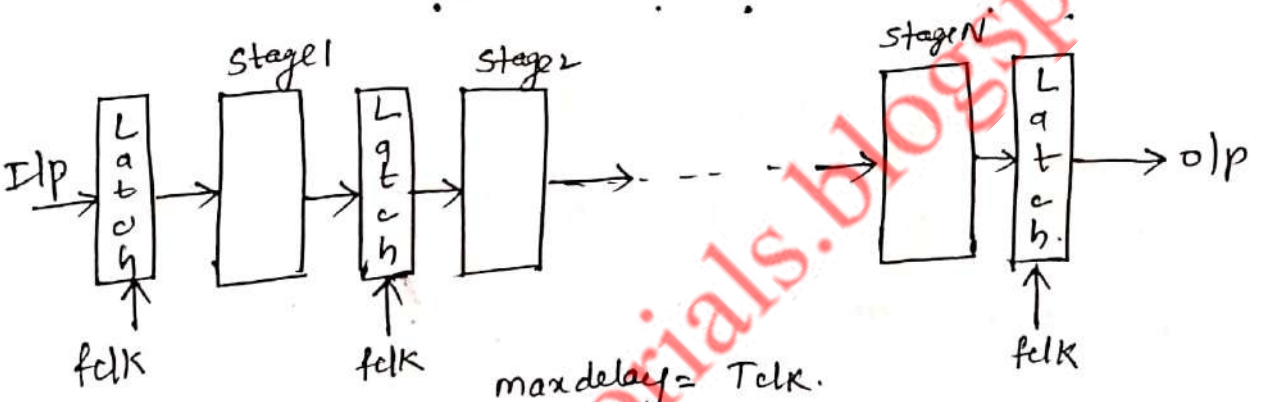
Observation:—

→ Using pipeling process same frequency is applied to latches, so speed is more and power dissipation is minimum. Hence low speed drawback of parallelism is overcomed.

Pipeling for 'N' stages:—

→ In 'N' stage pipeling process, different subtasks are performed by different hardware blocks known as stages.

→ The result produced by each stage is temporarily buffered in latches and then passed on to the next stage.



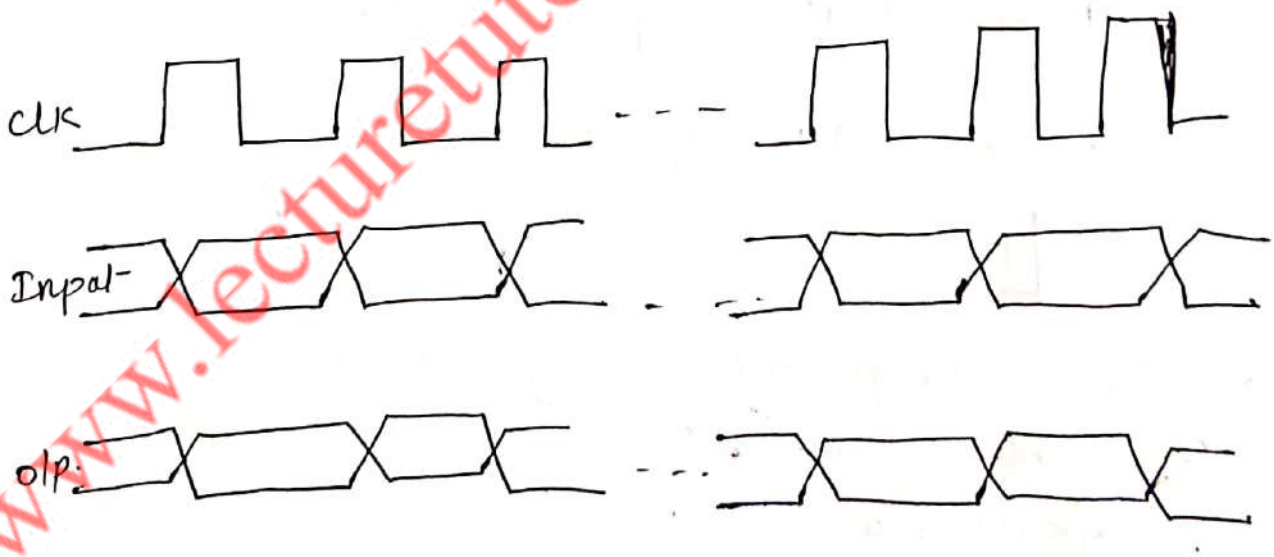


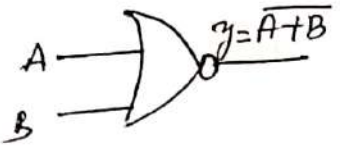
Fig:- N-stage pipeline structure & timing diagram.

Estimation and optimization of switching activity:-

Inorder to reduce power dissipiation, we can use lowering of switching activity and switched capacitance to a minimum level, there by we can have low-power design.

→ Concept of switching activity:- Switching activity is nothing but the no. of power consuming voltage transitions experienced by output capacitance per clock cycle.

Eg:- Let us consider a 2i/p NOR gate and the o/p transition probabilities as.



A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

Let P_0 – probability of o/p zero

P_1 – probability of o/p one.

P_{01} → probability of 0 to 1 transition power consumption

$P_{01} \Rightarrow P_0 \cdot P_1$

$P_{01} = \frac{3}{4} \times \frac{1}{4} = \frac{3}{16}$.

$P_0 = \frac{3}{4}$

$P_1 = \frac{1}{4}$

P_{10} → probability of 1 to 0 transition power consumption

$P_{10} \rightarrow P_1 \cdot P_0 = \frac{1}{4} \times \frac{3}{4} = \frac{3}{16}$.

The above transition probabilities can be shown with state transition diagram as

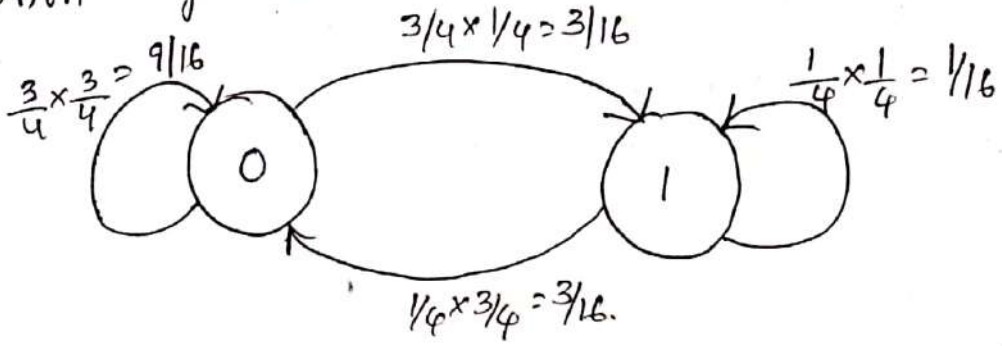


Fig:- State transition diagram & probabilities.

→ Switching capacitance:- The switching capacitance may be defined as:

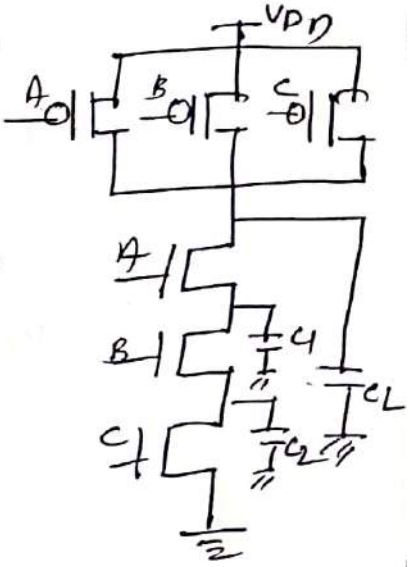
switching capacitance = switching activity X switched Capacitance

ie, The switching power dissipation can be minimized by minimizing switching activity / switching capacitance

→ power dissipation occurs due to load capacitance as well as at all internal node capacitances.

$$P_d = \alpha_{0\to L} V_{dd}^2 f + \sum_{i=1}^{K} \alpha_i C_i V_{dd}^2 f V_i$$

(V_i ↓ node voltage)



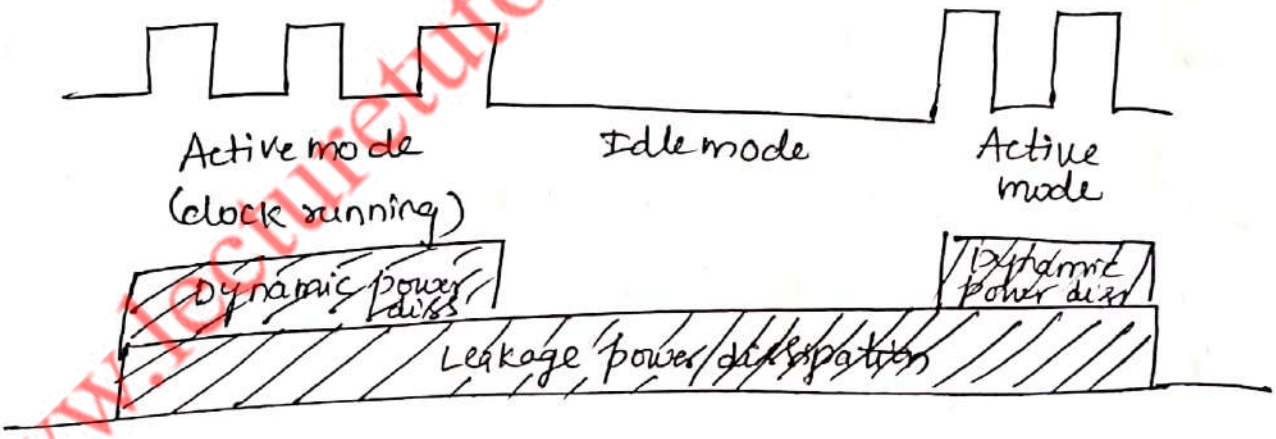
Methods of minimizing switching capacitance (or) Reduction of switching activity.

Includes
→ Gated clock signals (clock gating)
→ Glitch reduction
→ Signed magnitude representation.

Gated clock signals (clock gating):- It is one of the most successful and commonly used low power technique.

→ It is observed that large no. of transitions are unnecessary and such transitions can be supressed without affecting the functionality of circuit.

ie) Dynamically preventing the clock from propagating to some parts of the circuit under certain conditions.



To have a more knowledge on clock gating let us have two unsigned N-bit comparator as shown below.

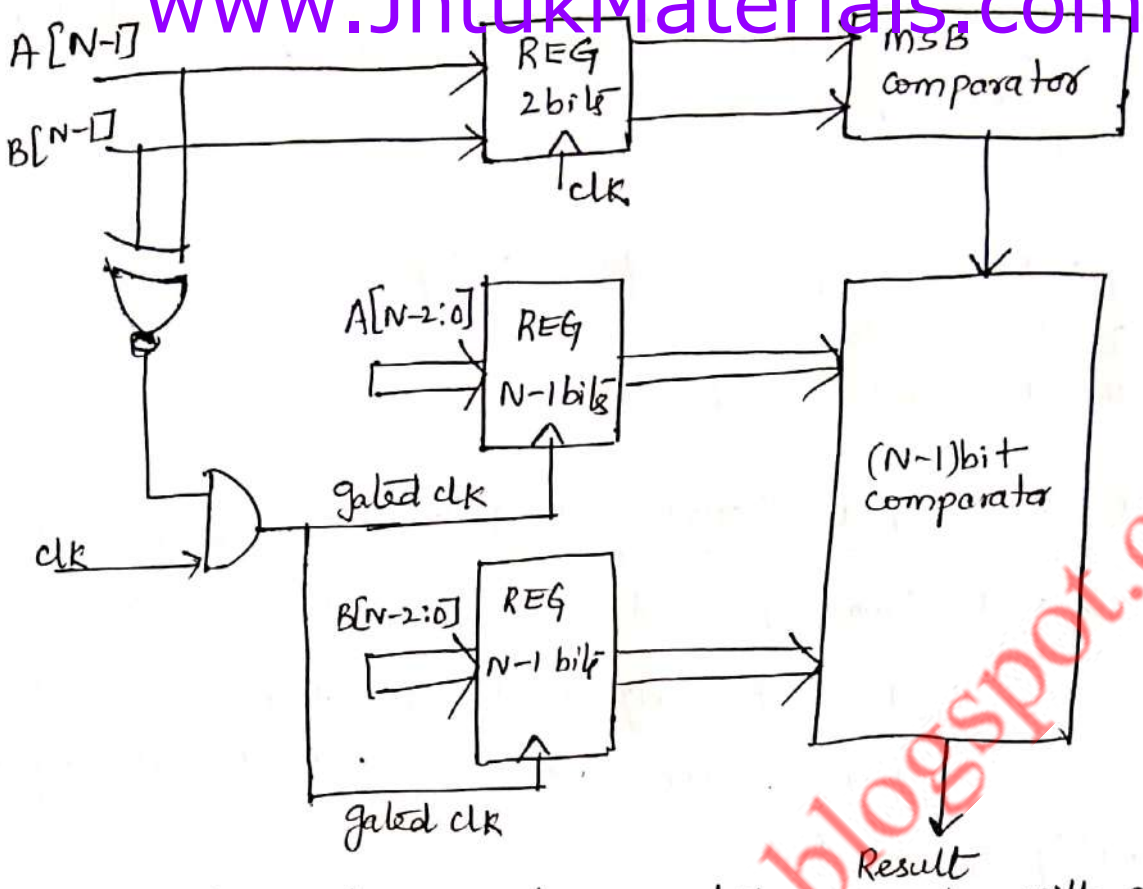


Fig: Block diagram of an N-bit comparator with gated clk

Operation:—

→ Two unsigned data bits are A[N-1:0], B[N-1:0] are applied.

→ Two MSB's of A & B are compared first with an application of clk signal.

→ If Both of MSB's are different, then o/p of XNOR is 0. means at the o/p of AND gate is '0'. Then no need to compare lower bits of A & B.

→ If MSB's of A & B are same, then we have to check lower bits of A & B [A(N-2:0), B[N-2:0], to decide which one is larger.

→ In that case o/p of XNOR is 1, then a gated clock will be applied through AND gate.

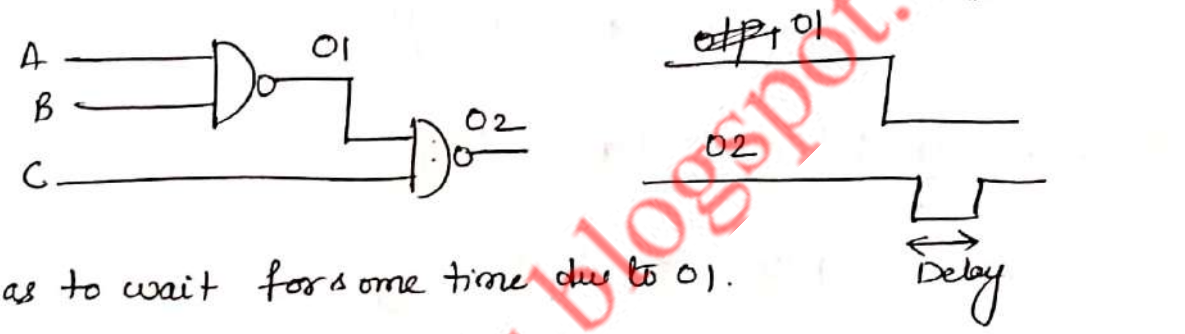
Conclusion:— There by this mechanism we can prevent application of clock for unnecessary blocks which will save power.

Glitch reduction:- When heavy currents are flowing through the chip lines of finite resistance, there may a voltage drop which will cause glitches.

→ These glitches may cause delay at the o/p of circuit and can contribute major dynamic power dissipation.

Note:- Heavy currents are due to short circuit power dissipation

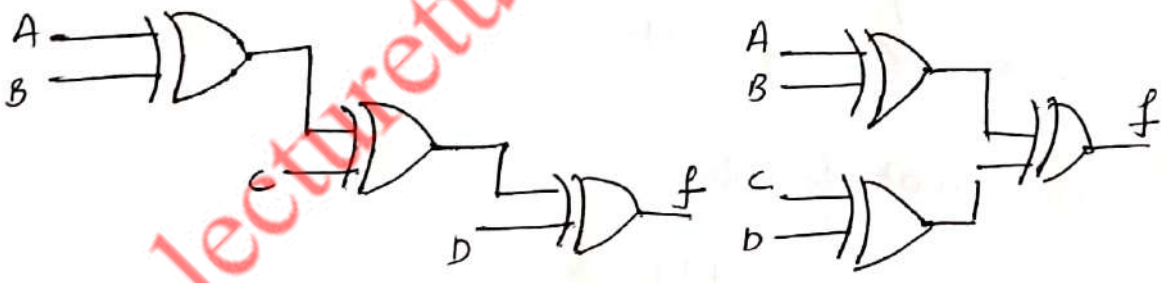
Eg:- The following example shows glitch at output 2



→ O2 has to wait for some time due to O1.

→ Glitching power can be minimized by the following techniques

* Balancing all signal paths
* Reducing logic depth



Chain structure

Balanced realization.

→ Sign-magnitude representation:-

In signed magnitude representation, for a given data, if MSB bit is 0, then it is +ve, if MSB is bit is 1, then it is -ve number.

ie; MSB '0' → +ve

MSB '1' → -ve

Eg:- +10 → MSB 0 1010

-10 → 1 1010

→ Sign extension for 8bit:-

+10 → MSB 0 0001010

-10 → 1 0001010

Drawback:- Sign-magnitude representation is not convenient. In implementing various arthamatic operations during computation so we use 2's complement

2's Complement of +10

+10 → 0 0001010

1's comp → 1 1110101

1

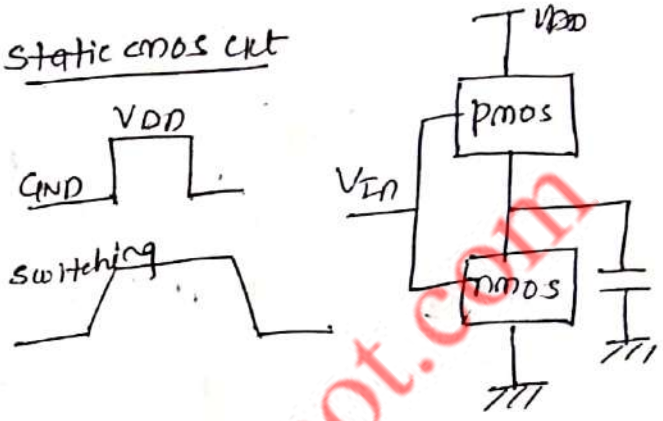
1

11110110

Adiabatic logic circuits

→ The term adiabatic is taken from thermodynamics theory, that refers, it donot release or take energy from outside environment

Static cmos ckt



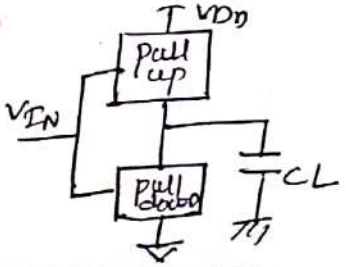
→ Full swing voltage mode cmos logic styles have been extremely successful both technically and interms of market share.

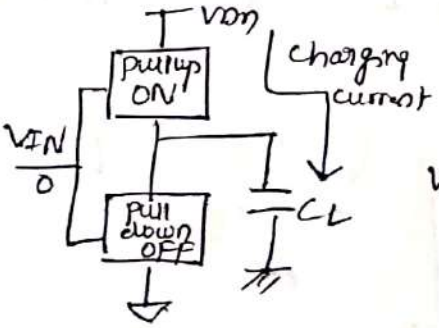
→ switching power dissipation of cmos circuit with capacitance load has a lower limit of $\frac{CLVdd^2}{2}$

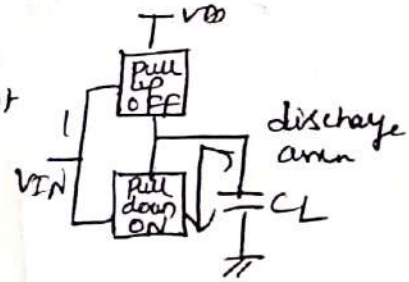
→ In Adiabatic switching circuit, the switching power dissipation is below lower limit of convential cmos logic.

→ The approach followed in adiabatic circuits is to recycle the energy, what ever energy has been transferred from the power source to the circuit, will be transfered back to power source after some computation done. That is why so called as reversable logic gates

→ switching power dissipation due to charging & discharging of load & parasitic capacitances.







The voltage across the capacitance as a function of time, $v_c(t)$ can be given as

$$v_c(t) = \frac{1}{C}\int_0^T i(t)\,dt \quad \text{over} \quad (0<t<T)$$

$$\int_0^T i(t)\,dt = I(t)\cdot T$$

$$v_c(t) = \frac{1}{C} I(t)\cdot T$$

$$\boxed{I(t) = \frac{v_c(t)\cdot C}{T}}$$

Avg current $0<t<T$

Energy dissipation in 'R' from 0 to T,

$$E_{diss} = \int_0^T i^2(t)\cdot R\,dt$$

$$\Rightarrow R\int_0^T i^2(t)\,dt$$

$$\Rightarrow R\, I(t)\cdot T$$

$$\Rightarrow R\,\frac{v_c^2(t)\,C^2}{T^2}\cdot T$$

$$\Rightarrow \frac{R C^2 v_c^2(t)}{T} \Rightarrow \frac{RC}{T} C v_c^2(t)$$

$$\boxed{E_{diss} = \frac{RC}{T} C v_c^2(t)}$$

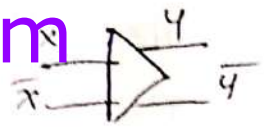
Case1 $\rightarrow$ $T = 2RC$

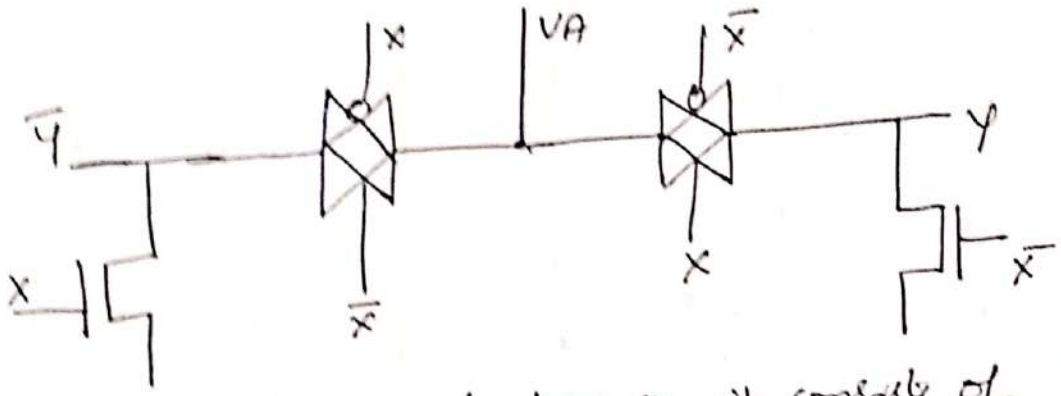
$$E_{diss} = \frac{RC}{2RC} C v_c^2(t) \Rightarrow \frac{1}{2} C v_c^2(t).$$

Case2 $\rightarrow$ $T > 2RC$, $E_{diss} < \frac{1}{2} C v_c^2(t)$.

Note:— when $T > 2RC$, Energy is reduced lessthan $\frac{1}{2} C v_c^2(t)$

Adiabatic amplification circuit





→ Adiabatic amplification circuit consists of 2 transmission gate and Nmos clampers.

→ Inputs and outputs are dual-rail-encoded to avoid the use of Cmos inverter

operation:- Depending on the valid input value, amplifier is energized by a slow voltage ramp from 0 to VDD.

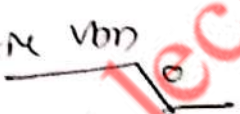
→ Next the amplifier is de-energized by ramping the voltage on VA back to 0. Keeping the input pair stable

→ During 

ramp, one of 'y' will be 1 and '$\bar{y}$' will be 0.

→ During 

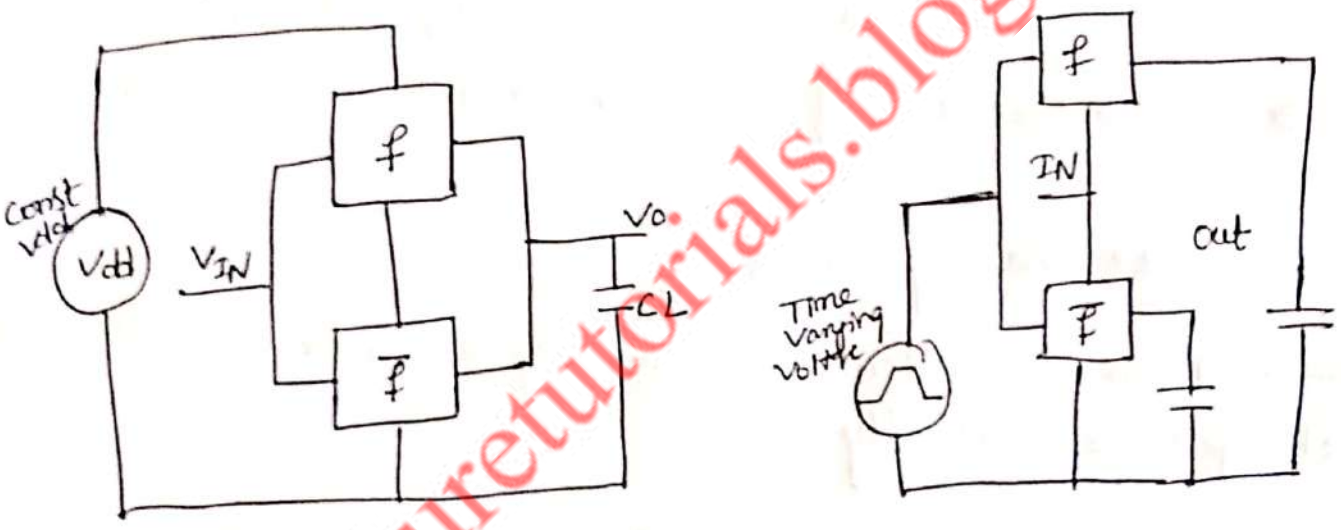
region, the o/p remain same

→ Pure 

ramp, the energy will be collected back to 'VA' which is called reversable operation.

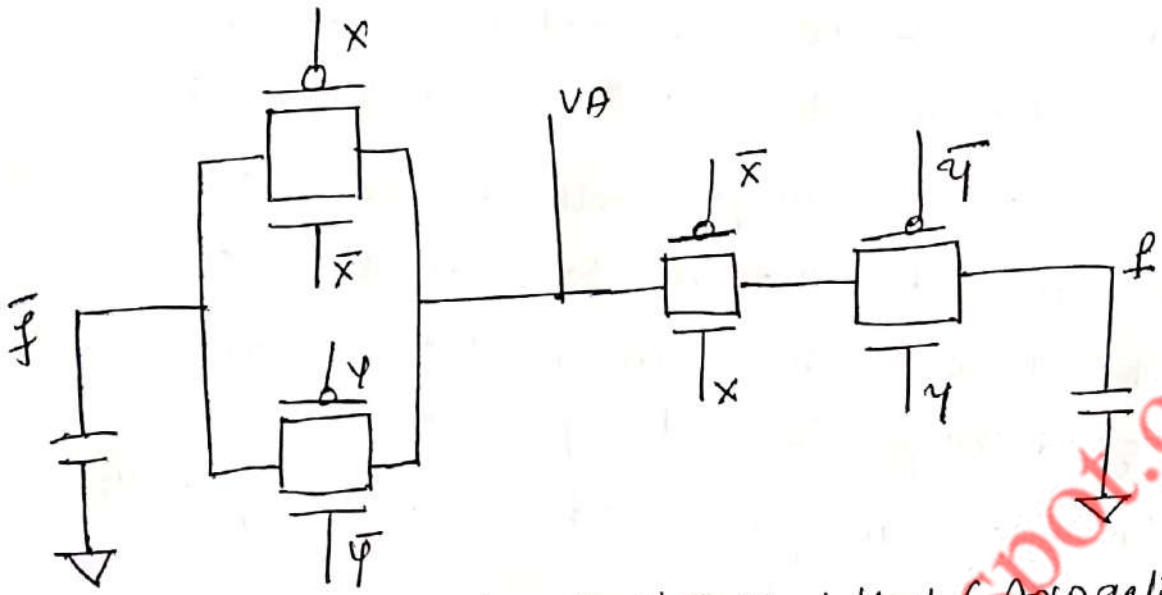
→ Realization of adiabatic gates:-

* Replace each of the pmos and nmos devices in the pullup & pull down network with Transmission gates
* use expanded pullup network to drive true output
* use expanded pull down network to drive complementary o/p
* Both networks in the transformed circuit are used to charge & discharge the load capacitance
* Replace DC VDD by a pulsed power supply with varying voltage to allow adiabatic operation



(a) Cmos (b) Adiabatic gate

Adiabatic AND/NAND gate:-



VA = f, when X = 1, Y = 1 (AND gate)

VA = $\bar{f}$, when X = 0, or Y = 0 or X & Y = 0 (NAND)

→ Draw back is no of transister are becoming doubled.

Stepwise charging circuit:-

→ These are alternative circuit by which the capacitor gets charged adiabatically.

Let us consider a convential cmos inverter with step wise increasing supply voltage as shown below

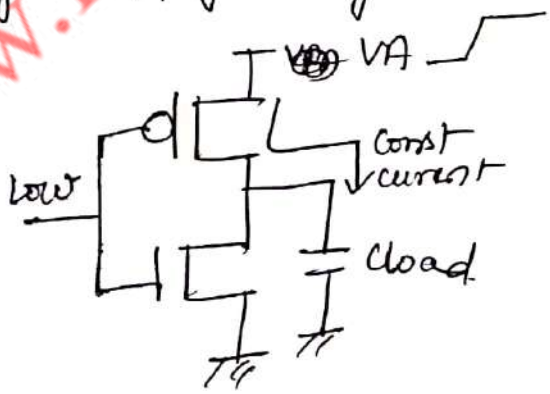
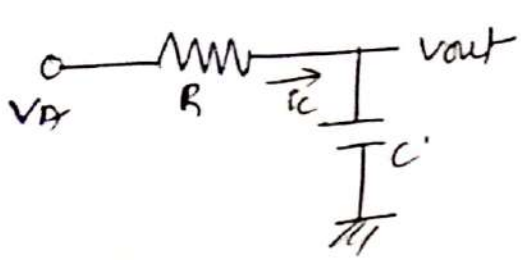


Fig:- cmos with step charging power

→ The equivalent circuit fa above one may be drawn as



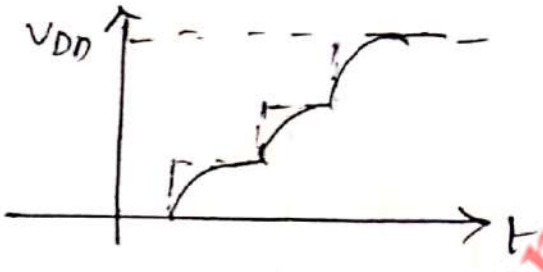
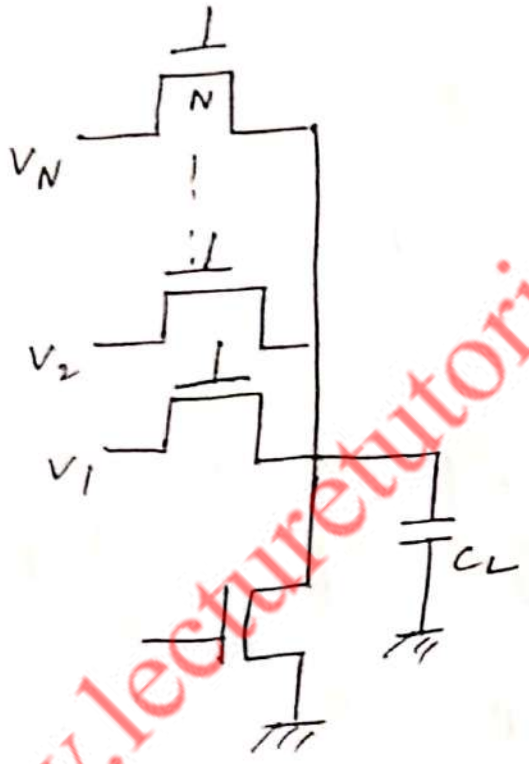
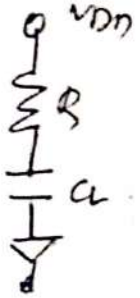


Fig:- Equivalent ckt & step charging.

For 'N' no. of MOSFETs the above circuit may be depicted as

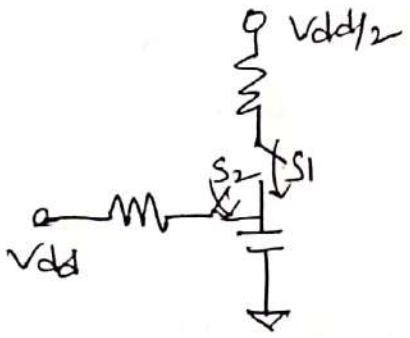


The power in one MOSFET can be given as



$$P = \frac{1}{2} C_L V_{dd}^2$$

→ For 2 MOSFETs [illegible]



$E = P = \frac{1}{2} C_L \left(\frac{Vdd}{2}\right)^2$

$\Rightarrow \frac{1}{2} C_L \frac{Vdd^2}{2^2} \Rightarrow \frac{1}{2N^2} C_L Vdd^2$ if $N=2$

∴ For 'N' no. of step charge ckts the power can be given as

$$E = P = \frac{1}{2N^2} C_L Vdd^2$$

Observation:— As 'N' increased (No. of steps), the power will get decreased.

Drawbacks:— → multiple supply voltages are required

→ overhead of routing many supply lines.

→ The energy per single step can be given as.

$E_{Step} = N \cdot E_{dis}$

$\Rightarrow N \cdot \frac{1}{2N^2} \cdot C_L Vdd^2$

$$E_{step} = \frac{1}{2N} C_L V_{DD}^2$$