Mos and Bicmos circuit design processes

Introduction:-

To design any circuit first of all we need to take the design considerations that is the specifications of the component of the system.

All those individual components are to be interconnected and metalizations are used to have a package circuit.

Mos layers:-

The basic mos layers that are used to design a circuit includes n^+ diffusions, p^+ diffusions, poly-silicon and etc..

Stick diagrams:-

Stick diagroms are outlined representations of layouts.

The stick diagrams convey the designing of the circuit through colour codes.

* For the designing of stick diagrams and layouts the MOS layers using colour codes are drawn as below.

For NMOS

S.No	layer	color	stick diagram representation	layout representation
1.	n^+ diffusion	Green		
2.	p^+ diffusion	yellow		
3.	Polysilicon	Red		
4.	Metal	Blue		
5.	Ion implantation	yellow		
6.	Burried contact	Brown		
7.	Contact cut	Black		
8	Supply lines	Black	X	
9.	Demarkation line	Brown		

For PMOS:-

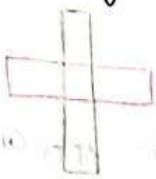
for pmos designing the only charge is ion implantation.

S.No.	layer	color	stick diagram representation	layout representation
1.	Ion Implant -ation	green		

Mos transistor representations:-

NMOS Enhancement

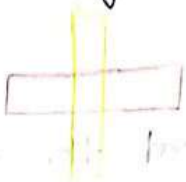
Stick diagram



layout

PMOS Enhancement

stick diagram



layout

NMOS depletion mode

Stick diagram

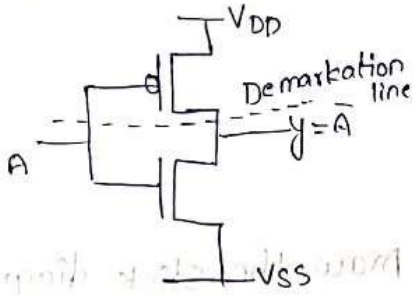
layout

PMOS depletion mode

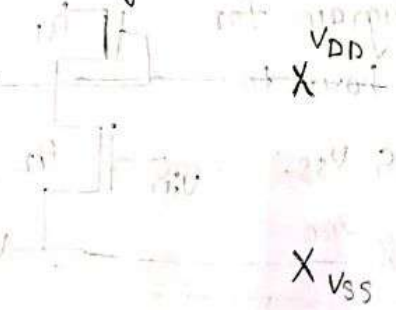
stick diagram

layout

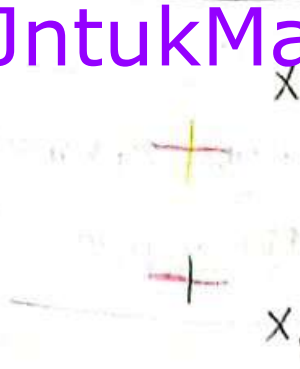
1. Design a stick diagram for Cmos inverter:-



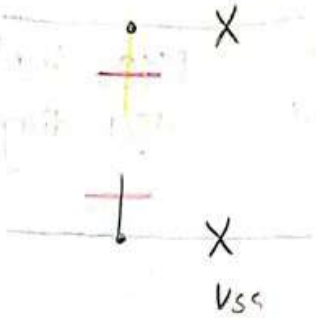
Step 1:- To design a cmos inverter, first we have to draw the supply lines V_{DD} and V_{SS}



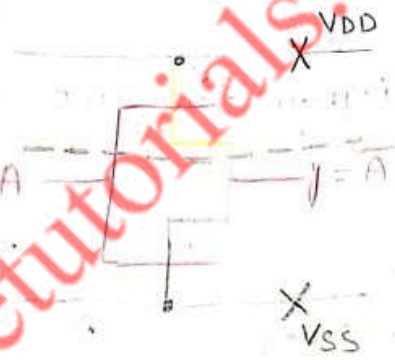
Step 2:- After V_{DD} and V_{SS} place the required transistors at a given place.



Step 3:- extend the transistors towards V_{DD} and V_{SS} and make contact cuts

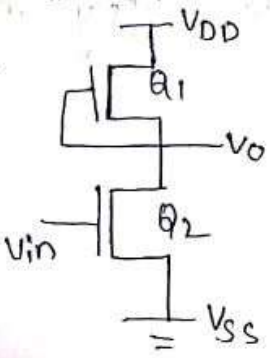


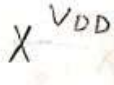
Step 4:- finally take i/p and o/p terminals

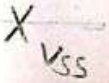


Q. Draw the stick diagram for nmos inverter:-

Step 1: To draw stick diagram for nmos inverter first we have to draw supply lines V_{DD} & V_{SS}.

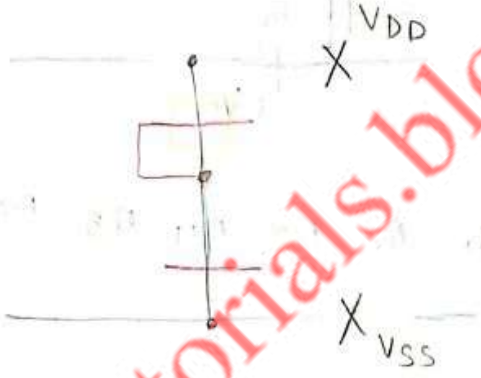




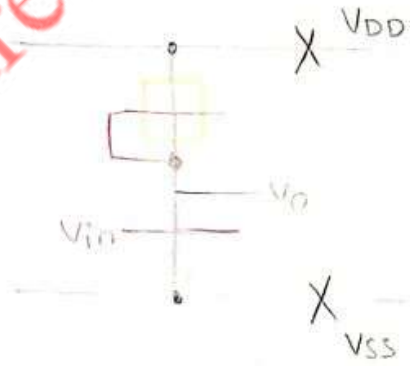


Step2:- After drawing supply lines place the required transistors.

Step3:- extend the transistor lines toward VDD and Vss and place contacts and Buried Contact



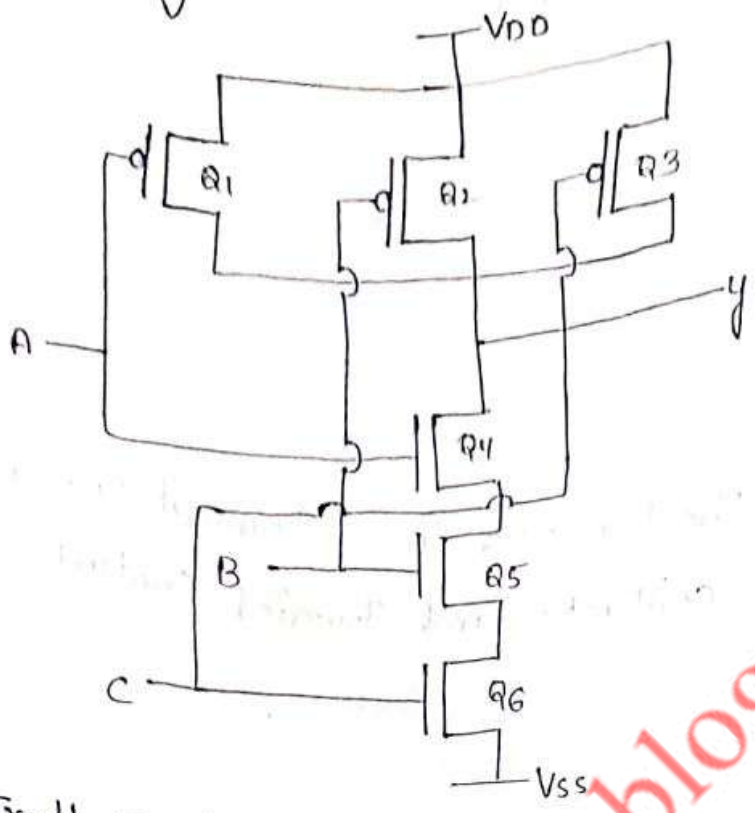
Step4:- finally take i/p and o/p's terminals.



3. Draw stick diagram for three input NAND gate using cmos technology.

	Nmos	pmos
NAND	series	parallel
NOR	parallel	series

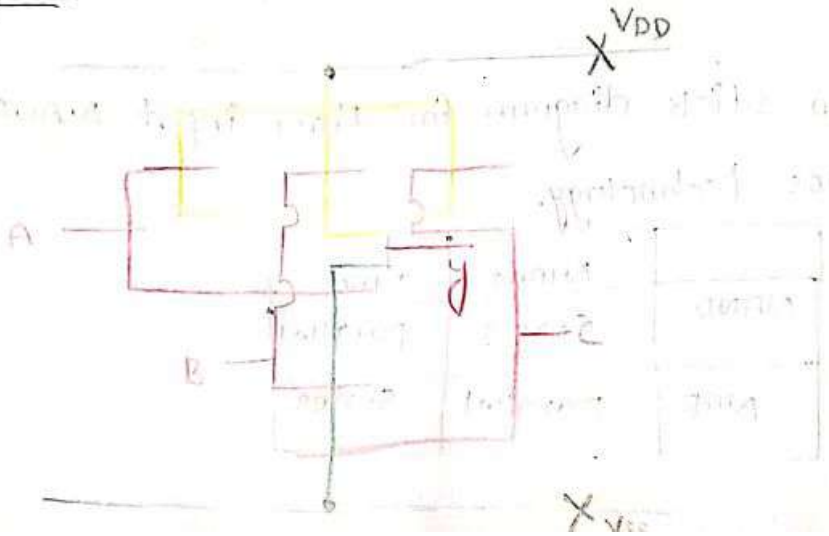
Circuit diagram



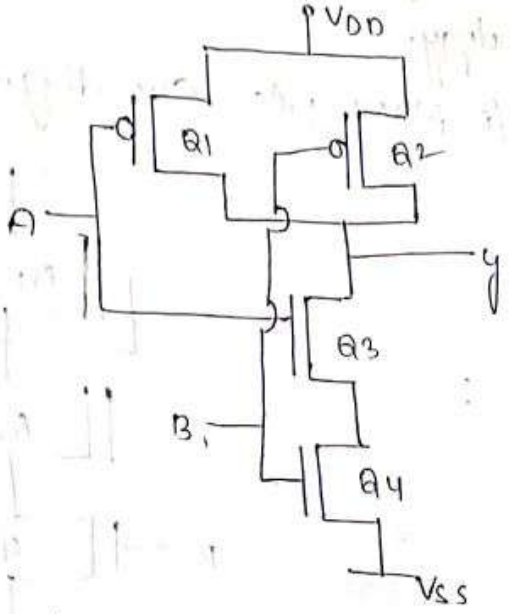
Truth Table

A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	y
0	0	0							
0	0	1							
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

Stick diagram:-

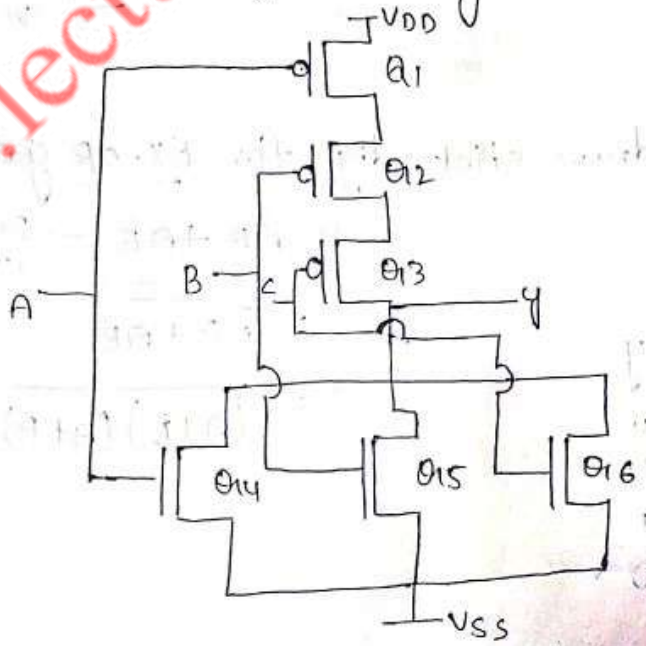


4. Draw the 3 i/p NAND gate using cmos technology



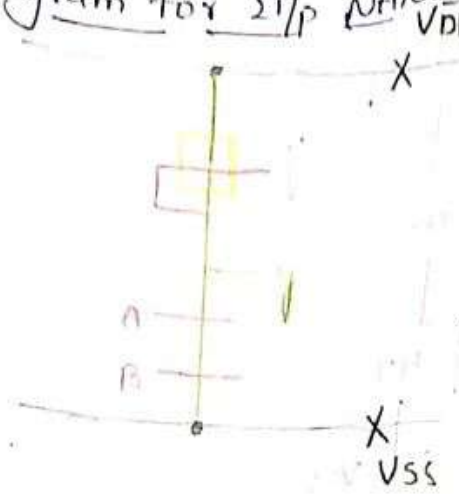
stick diagram:-

5) Draw 3 i/p NOR gate using cmos technology

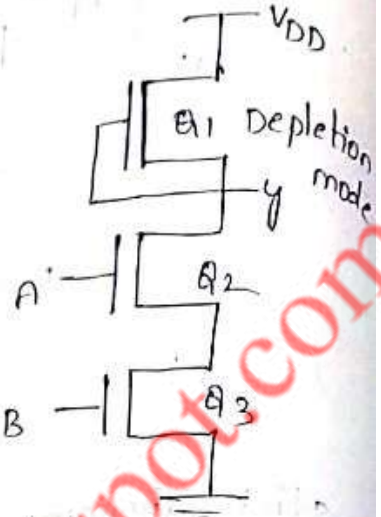


6) Draw the stick diagram for 2 i/p NAND gate using Nmos technology.

Stick diagram for 2i/p NAND gate

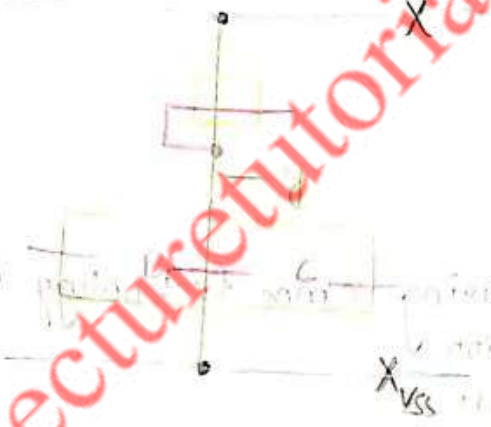


Ckt diagram

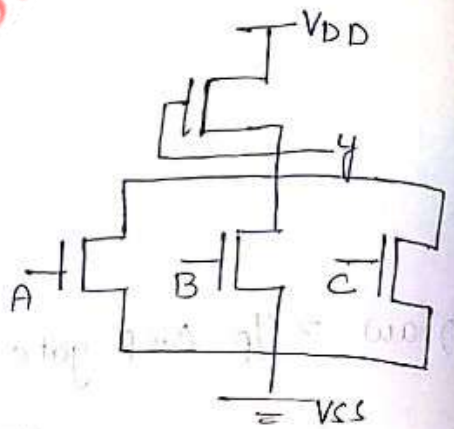


7) Draw the 3i/p NOR gate using Nmos technology

Stick dig for 3i/p NOR gate:-



Ckt diagram



8) Desig and draw stick dig for EX-OR gate

Truth Table

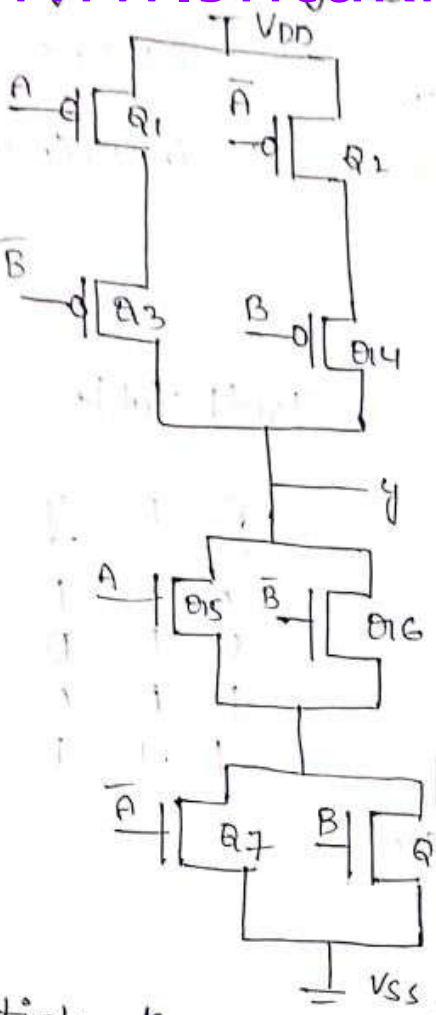
A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

$y = A\bar{B} + \bar{A}B$ — Boolean expression

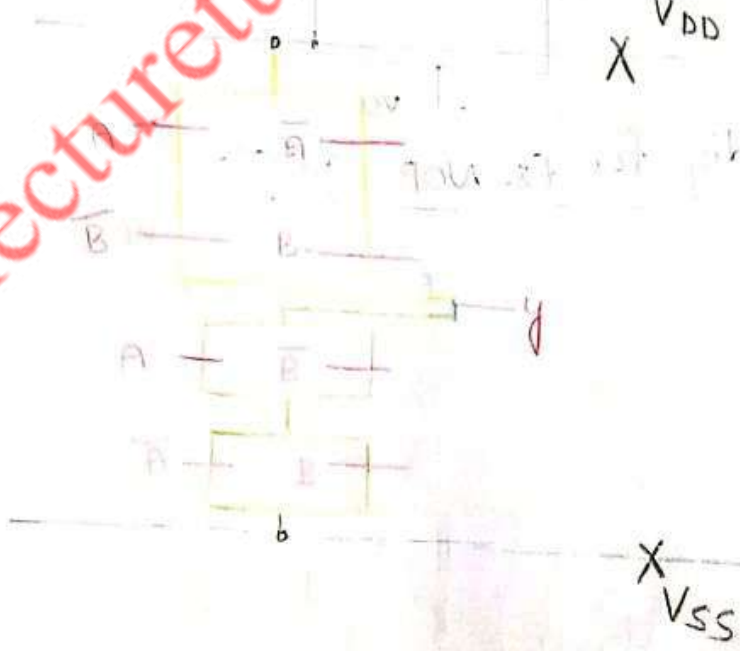
$= \overline{\overline{A\bar{B}} + \overline{\bar{A}B}}$

$= \overline{(\bar{A}+B)(A+\bar{B})}$

Ckt dig for Ex-or gate



Stick diagram for Ex-or gate:-



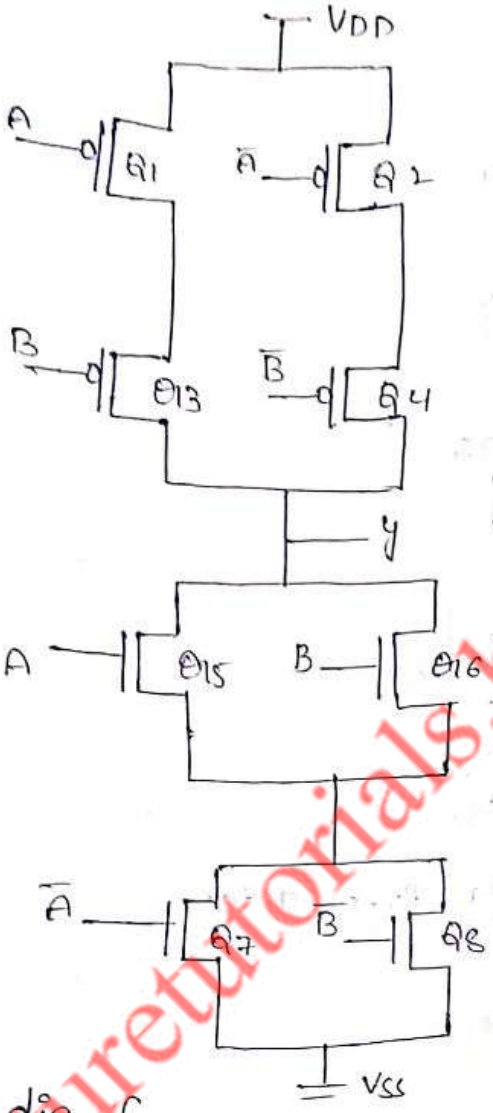
9) Design ckt for Ex-NOR gate

$y = \bar{A}\bar{B} + AB$

$= \overline{\bar{A}\bar{B} + AB}$

$= (A+B)(\bar{A}+\bar{B})$

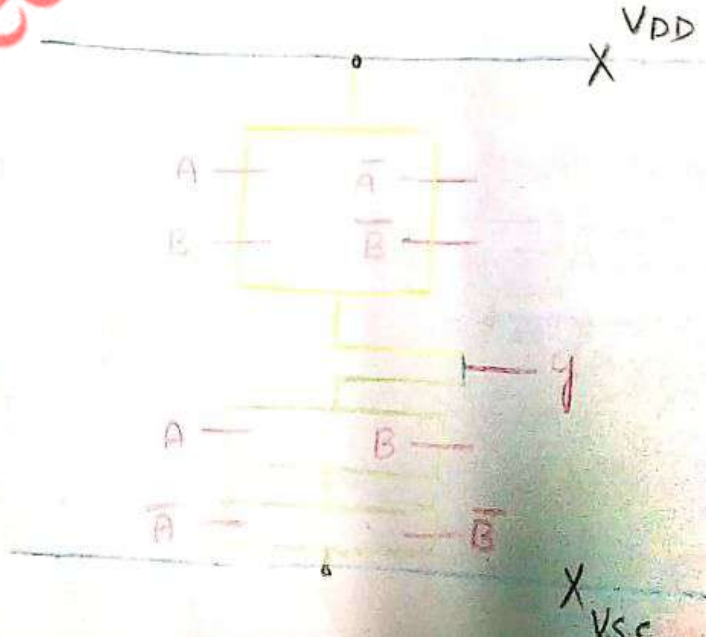
Ckt dig for Ex-NOR gate:-



Truth table

A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

Stick dig for Ex-NOR gate:-



Design rules and layout

* As the complexity of VLSI technology is more and more to have better understanding we are using a set of rules called Design rules.
* The design rules are the effective interface b/w Design Engineering and fabrication Engineering
* Ckt designers in general want tighter, smaller layouts for improved performance and reduced silicon area.
* The process Engineer want's Design rules that result's in a controlable and reproducee process.
* So, we need to have compromise b/w ckt design-er and process engineer requirments.
* Basically we are having two types of design rules
  1. Scalable Design rules ('λ' base)
  2. Absolute Design rules (micron base)

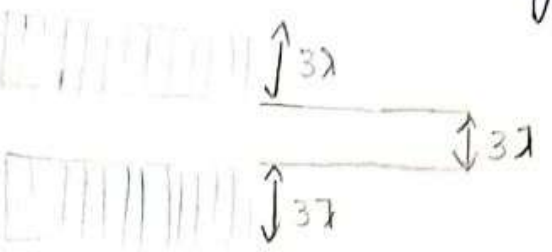
Scalable Design rules:-

1. The minwidth of metal 1 is 3λ and spacing b/w metal 1 and metal 1 is 3λ.
2. The minwidth of metal 2 is 4λ and spacing b/w metal 2 & metal 2 is 4λ.
3. The minwidth of n^+ diffusion (or) p^+ diffusion is 2λ and spacing b/w n^+ diffusion to n^+ diff & p^+ diffusion to p^+ diffusion is 3λ.

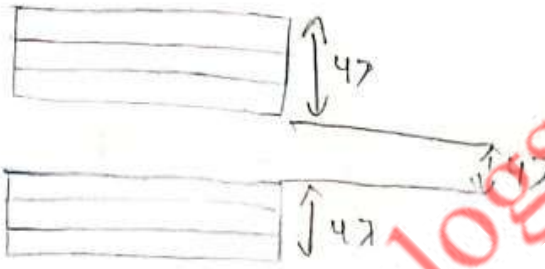
4. The minimum width and spacing for polysilicon to polysilicon is 1λ.

Min width Min spacing

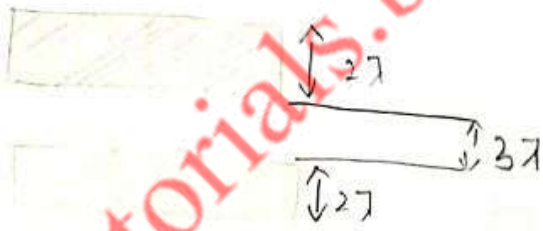
Metal 1:



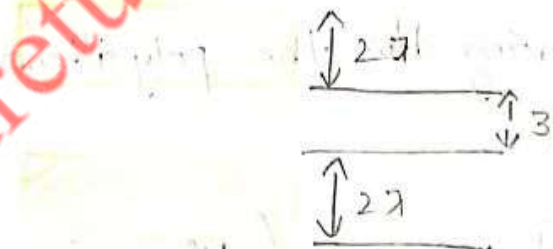
metal 2:-



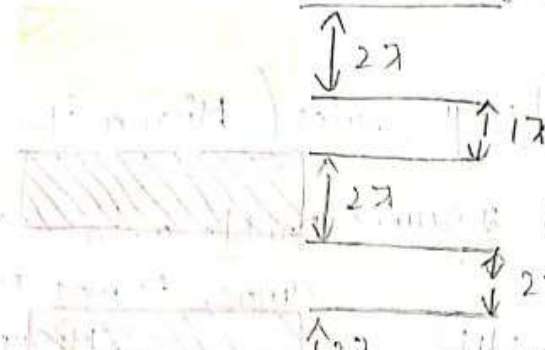
n^+ diffusion :



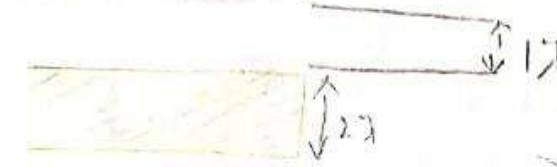
p^+ diffusion:



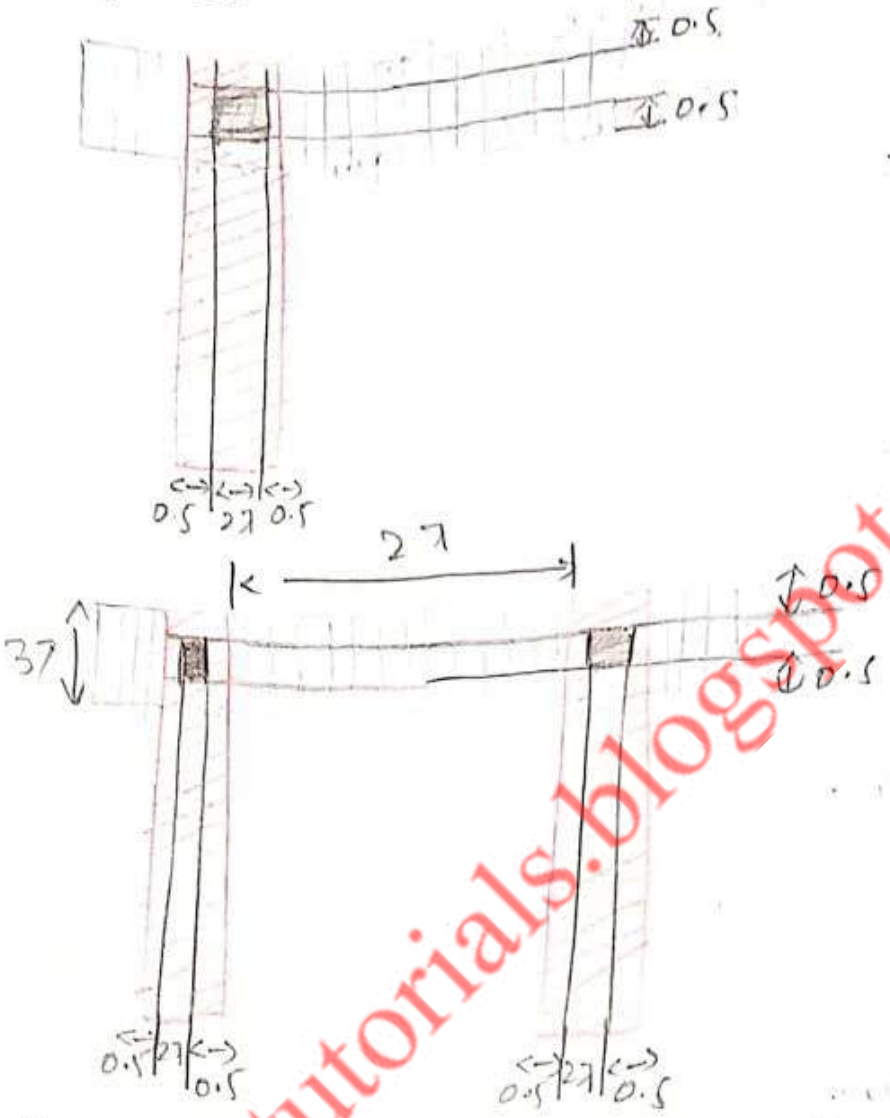
poly silicon :



n^+ diffusion :



Contact cut



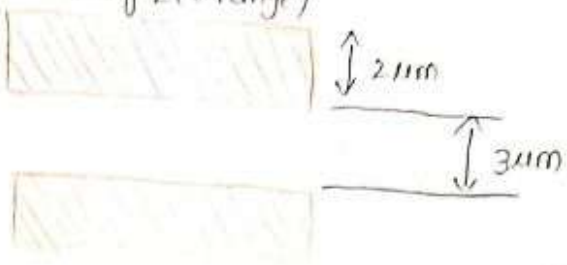
The spacing blw the poly silicon 1 & polysilicon 2 is 2λ.

Absolute Design Rules (Micron Base):-

1. 2μm and 2.5μm (Double metal ; Double poly):-
cmos, bicmos processes

Minwidth	Minspacing

Poly 2 (orange)

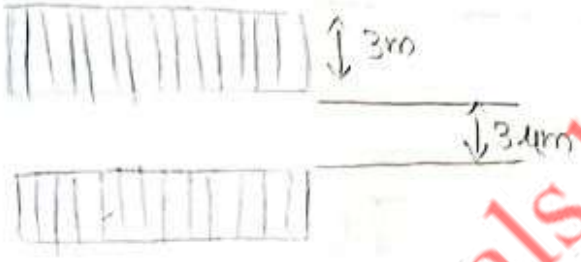


$P^+/n^+ \rightarrow P_1 \rightarrow 1\mu m$

$P^+/n^+ \rightarrow P_2 \rightarrow 1.5\mu m$

$P_1 \rightarrow P_2 \rightarrow 2\mu m$

Contact 2



$P_1 m_1$

$P_1 \rightarrow 2\mu m$ & $2.5\mu m$

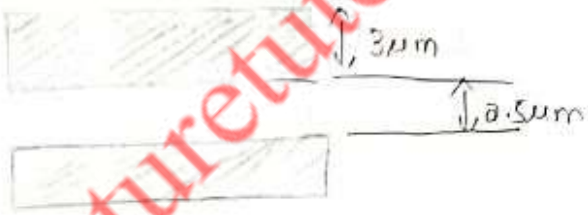
$m_1 \rightarrow 2\mu m$ & $2.5\mu m$

$P_2 \rightarrow 2\mu m$ & $3\mu m$

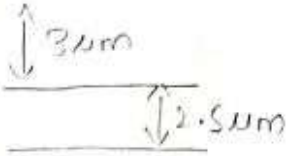
$m_2 \rightarrow 3\mu m, 3\mu m$

$P^+/n^+ \rightarrow 3\mu m$ & $2.5\mu m$

n^+ Diff



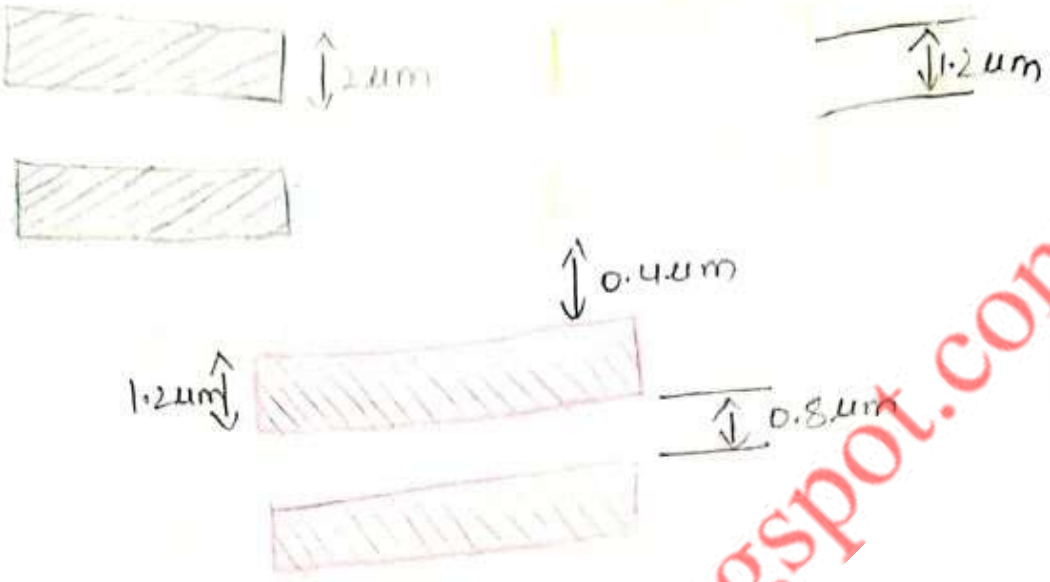
P^+ Diffusion



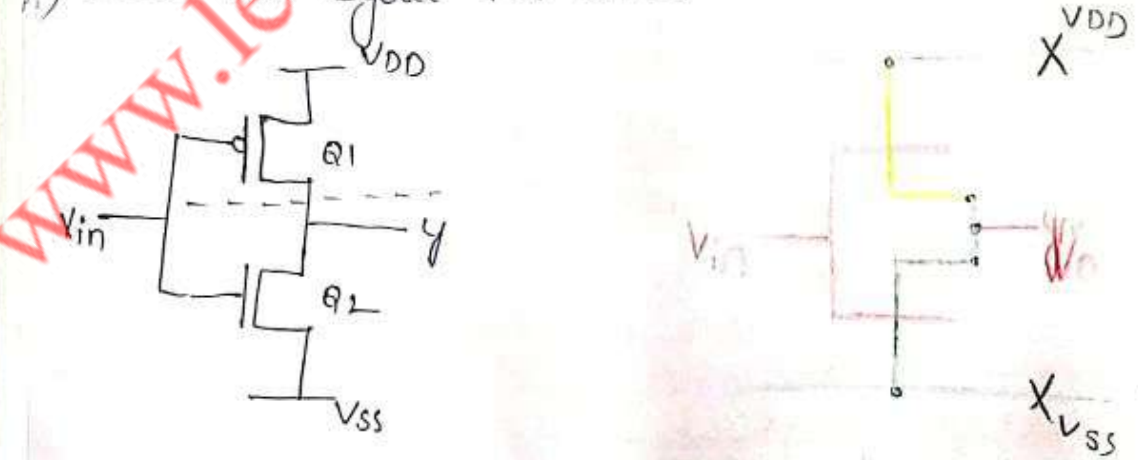
1.2μm (Polysilicon gate poly):-

Minwidth

Minspacing



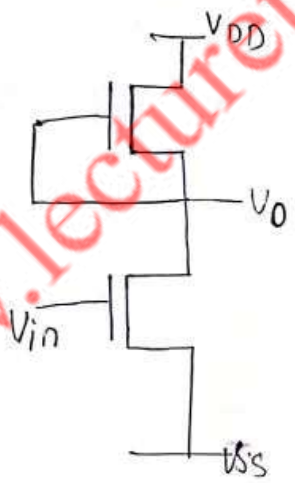
1) Draw the layout for Cmos inverter.

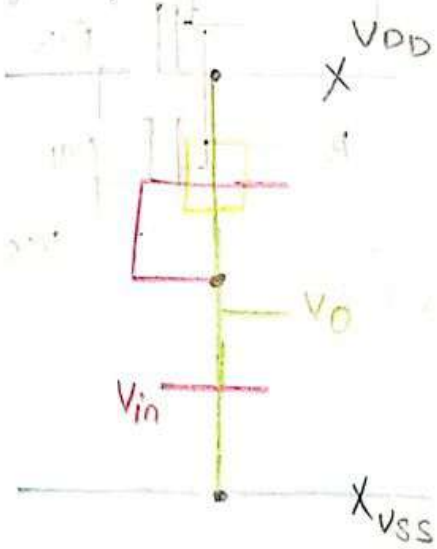


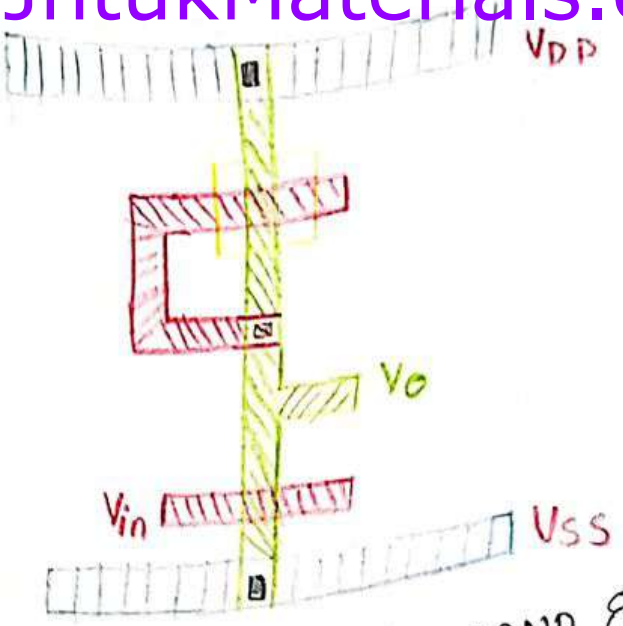
CMOS inverter ckt

2) Draw the layout for nmos inverter.

Nmos inverter ckt

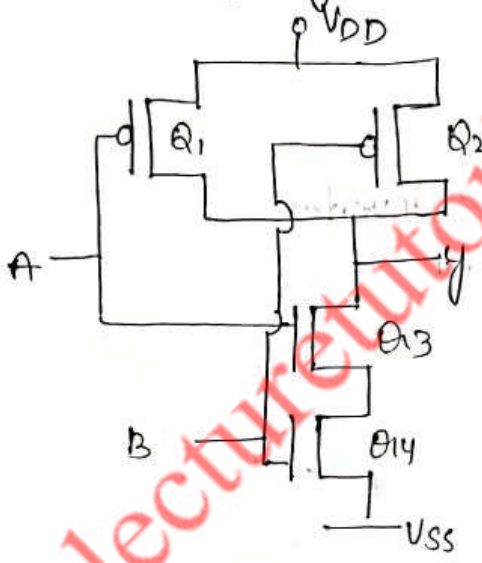




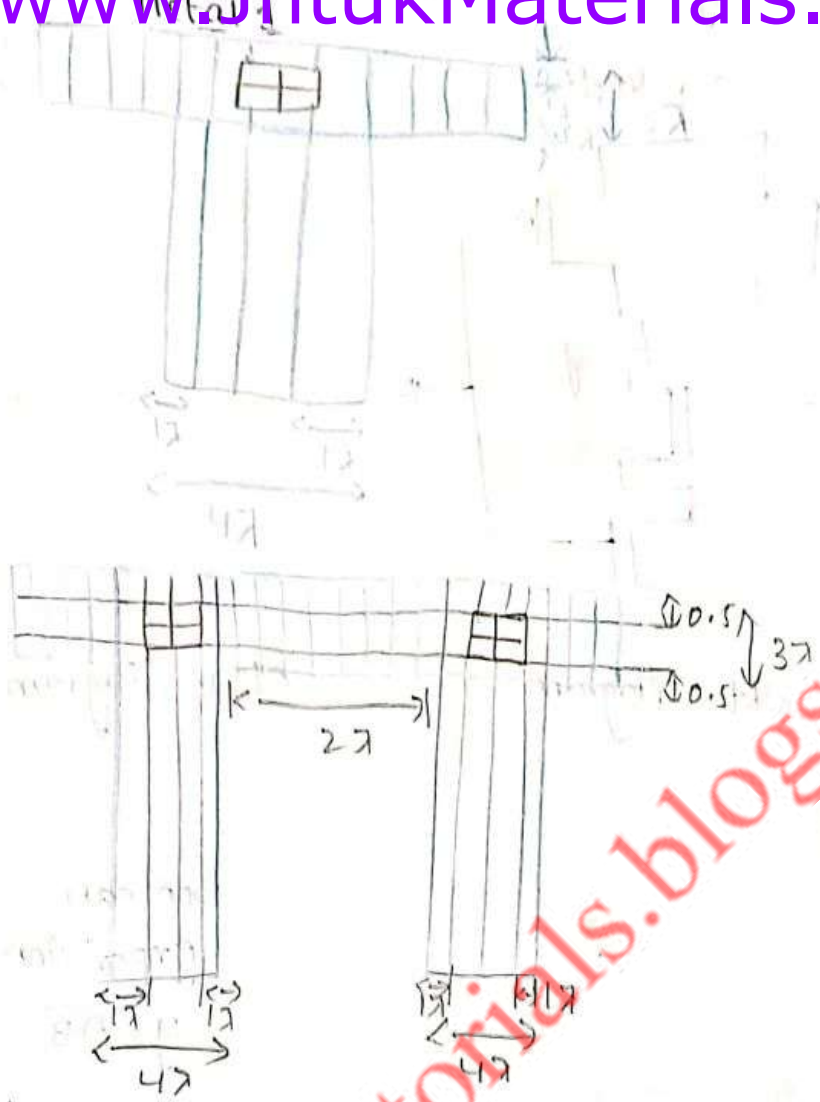


* Draw the layout for 2 i/p NAND gate using Cmos logic.

A. Circuit Diagram



Via

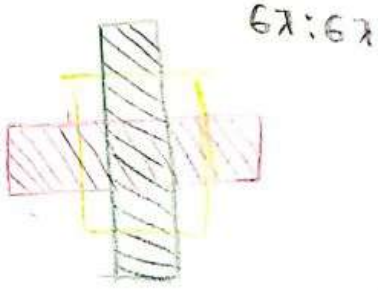


The spacing b/w via 1 & via 2 length is 2λ

Transistor representation:-

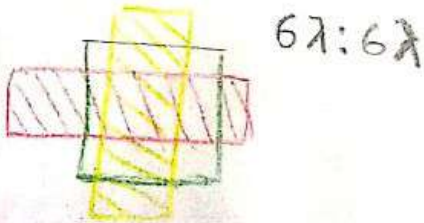
nmos enhancement

nmos Depletion

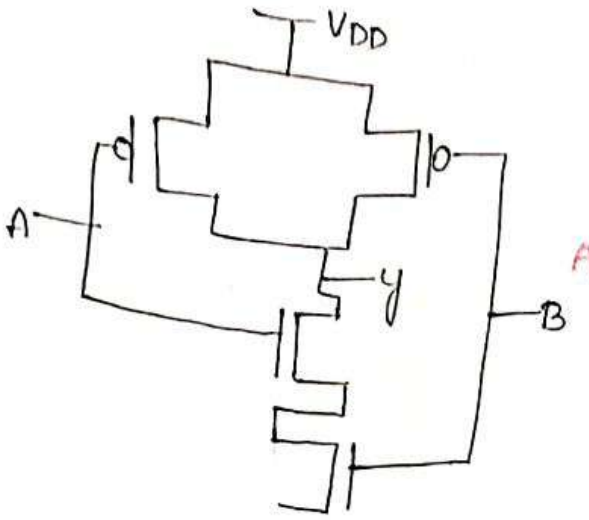


pmos enhancement

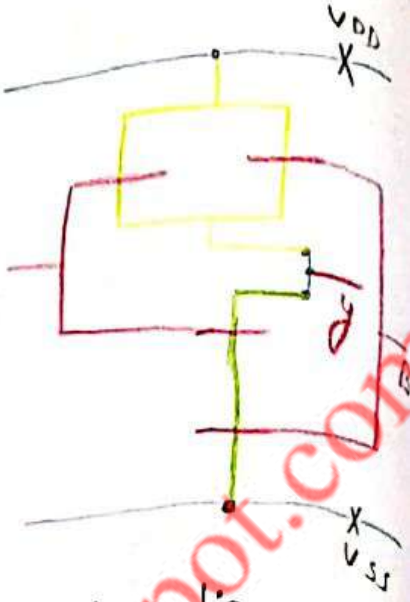
pmos depletion



* Draw the layout for 2 i/p NAND gate using cmos logic.

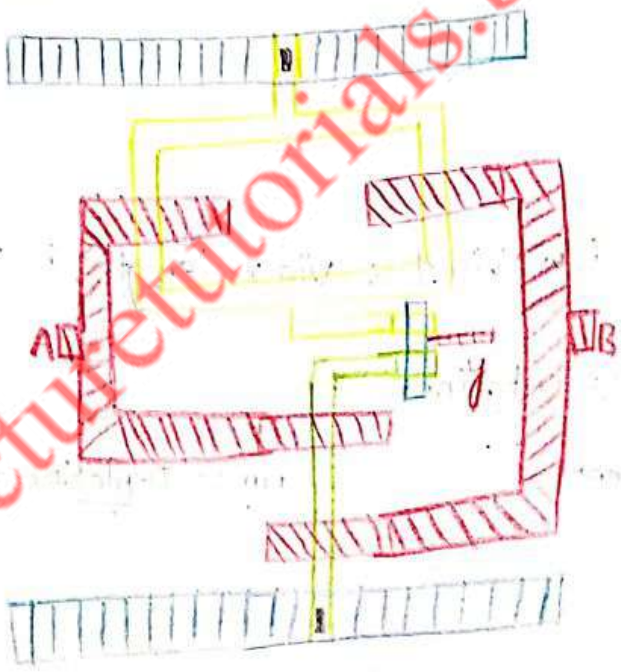


ckt diagram



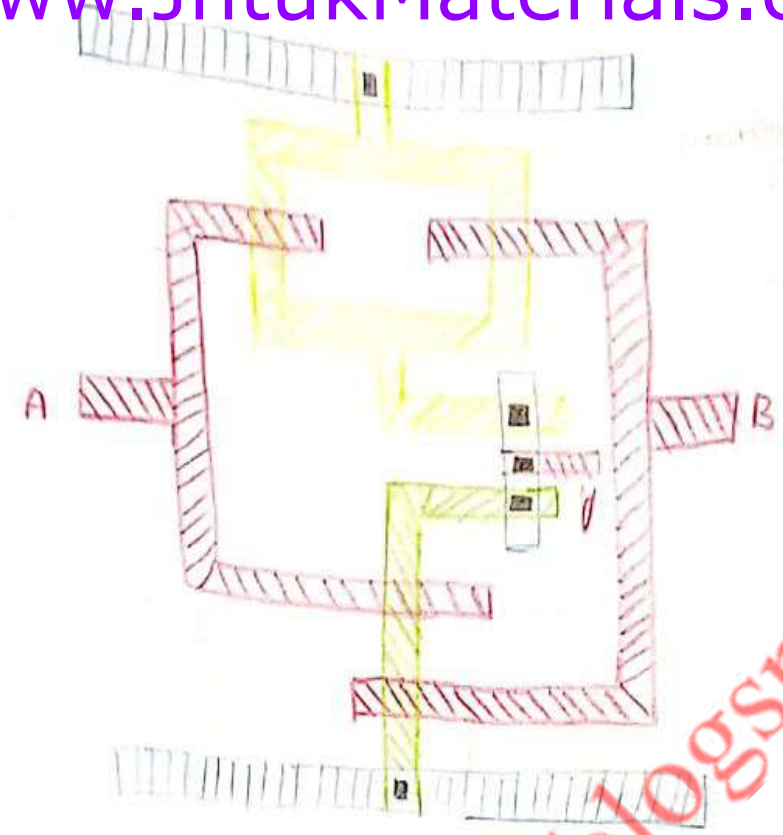
Stick diagram

layout



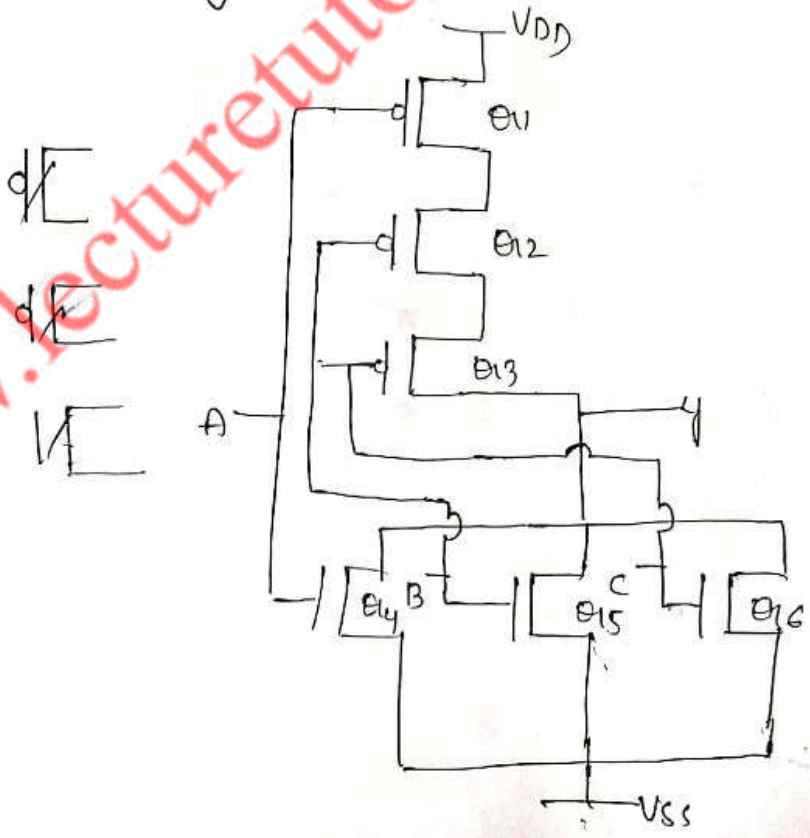
boolean expression

$y = \overline{AB}$

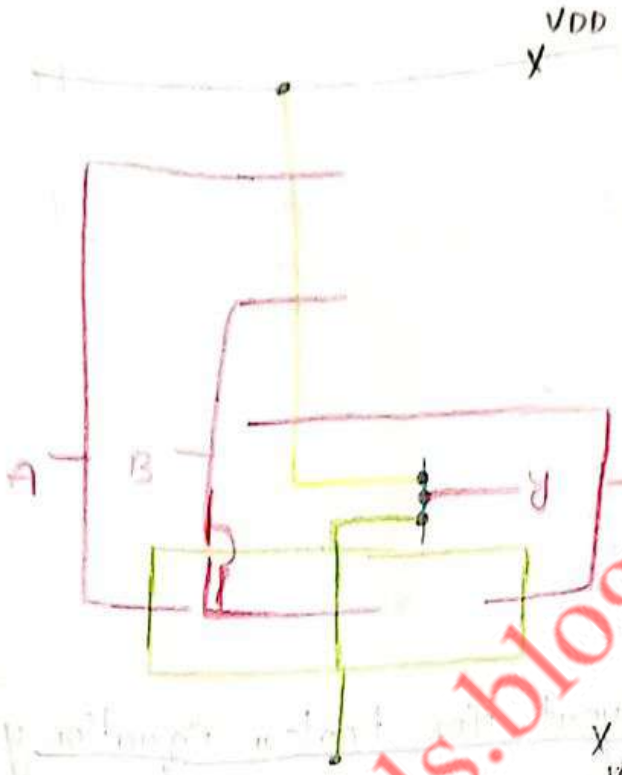


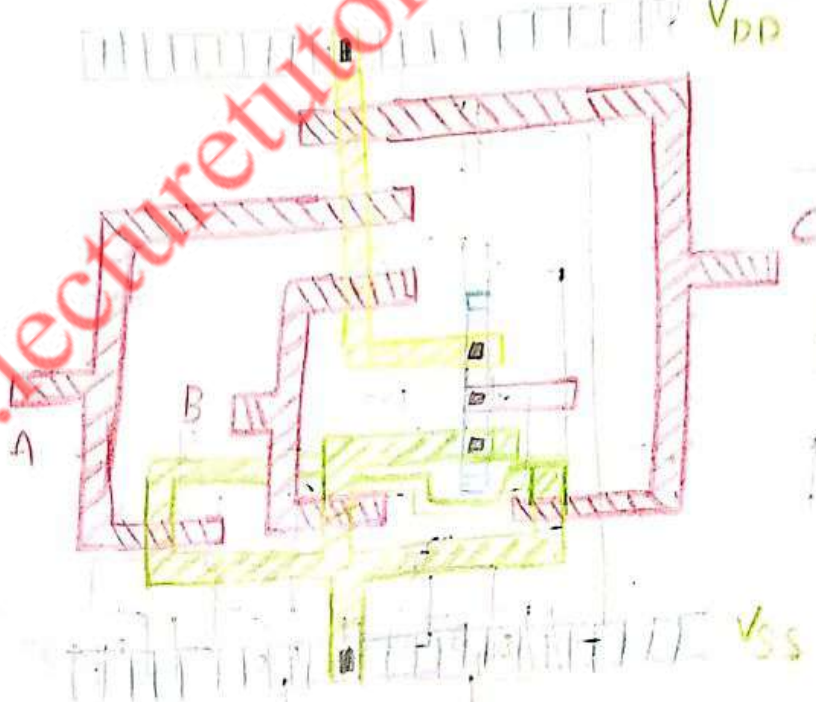
*Draw the layout for boolean equation $y=\overline{(A+B+C)}$ using cmos logic.

A. Circuit Diagram



General Stick diagram

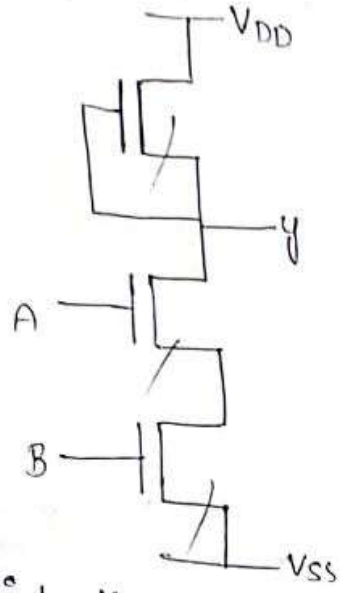


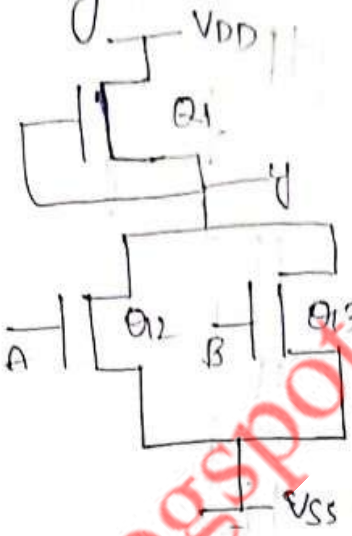


→ 2 i/p NOR gate using nmos logic → $y = \overline{A+B}$

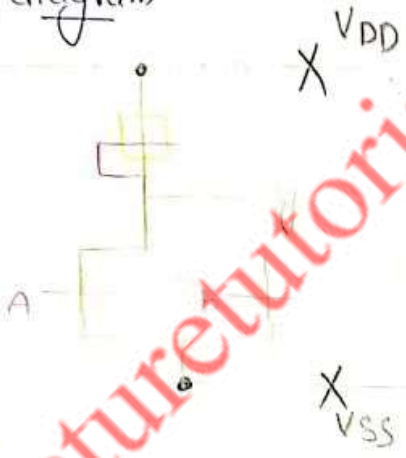
→ 3 i/p NAND gate using nmos logic → $y = \overline{ABC}$

1. 2 i/p NOR gate using nmos logic.





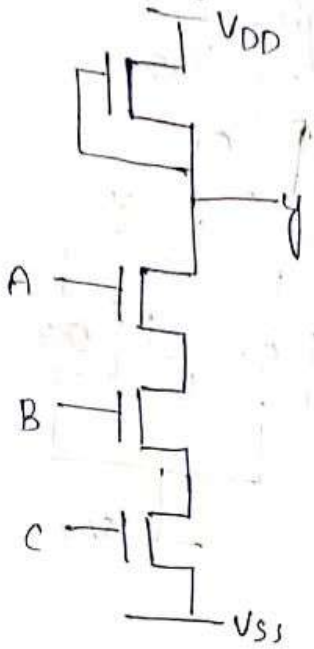
Stick diagram



Layout

* 3 i/p NAND gate using nmos logic. $y = \overline{ABC}$

Circuit diagram



Stick diagram

Layout

General observations about design rules:

A VLSI designer is dealing with silicon circuits whose dimensions and features are extreamly microscopic in nature.

* If the line widths are to small, the lines so define may tend to be discontinuous case places (or) may accordingly merge at places.

* The main purpose of design rules are

1. provides Communication links between circuit designer and process Engineer responsible for fabrication.
2. The goal of any set of design rules should be optimise yield while keeping the geometry as small as possible without Compromising the realibity of the finished circuit.
3. Try to exculed poly from the areas of p+mask/ n^+ mask that may Effect the resistance of poly at certain paths.
4. Metal is depoisted at the top of all oxide layers, Since it is light reflective, these factors combine poor edge defination.
5. Metal 2 is having even more unevent terrains on which to be depoisled and patterend. Hence metal 2 is wided than metal 1.
6. metal to metal seperation is also large and is brought above mainly by difficulties indefining metal edges.