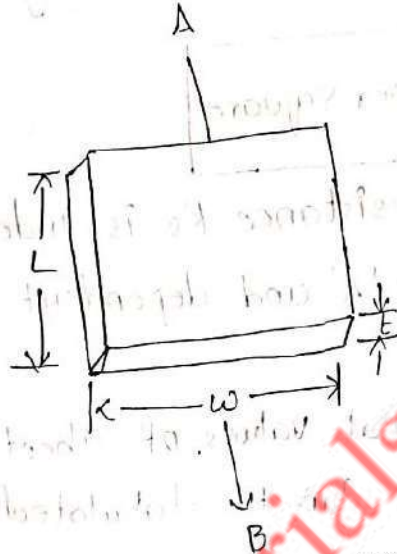


Sheet Resistance (R_s)

The Concept of Sheet Resistance can be understood by considering a uniform slab material as shown in the figure below.



Sheet Resistance Model

* So from the given diagram we can say that it is having a length of ' L ' and width of ' w ' and with a thickness of ' t '.

* The Resistance b/w the terminals A and B can be given as R_{AB} .

$$R_{AB} = \frac{\rho L}{A}$$

Where ρ - resistivity

L - length of the material

A - cross-sectional Area

* For a uniform slab $L=w$

$$WKT \quad R_{AB} = \frac{\rho L}{A}$$

$$R_{AB} = \frac{\rho l}{A}$$

$$R_{AB} = \frac{\rho l}{wt}$$

$$= \frac{\rho l}{wt} \quad (\text{uniform slab } l=w)$$

$$R_{AB} = \frac{\rho}{t}$$

∴ The sheet Resistance R_s can be given as

$$R_s = \frac{\rho}{t} \quad \Omega \text{ per square}$$

Note:- The sheet Resistance R_s is independent of Cross-sectional Area 'A' and dependent on thickness 't'.

* Some of the typical values of Sheet Resistance of different technologies can be tabulated as like below

Layer	sheet Resistance		
	5μm	2μm (orbit)	1.2μm
Metal	0.03	0.04	0.04
Diffusion (Active)	10→50	20→45	20→45
silicid side	2→4		
polysilicon	15→100	15→30	15→30
n-transistor channel	10 ⁴	2×10 ⁴	2×10 ⁴
p-transistor channel	2.5×10 ⁴	4.5×10 ⁴	4.5×10 ⁴

Resistance Concept Applied to MOS Transistors

Sheet Inverters:-
The sheet Resistance Concept can be extended to inverters.

Here let us consider a CMOS inverter as shown below.

* The channel Resistance of pmos can be given as

$$R_{pus} = Z R_s$$

$$\text{WKT } Z = \frac{L}{W}$$

$$\Rightarrow \frac{2\lambda}{2\lambda} = 1$$

$$R_{pus} = 1 \cdot R_s$$

$$= (2.5 \times 10^4)$$

$$R_{pus} = 25 \text{ k}\Omega$$

* The channel resistance of nmos can be given as

$$R_{pds} = Z \cdot R_s$$

$$Z = \frac{L}{W}$$

$$= \frac{2\lambda}{2\lambda} = 1$$

$$R_{pds} = 1 \cdot R_s$$

$$= 1(10^4)$$

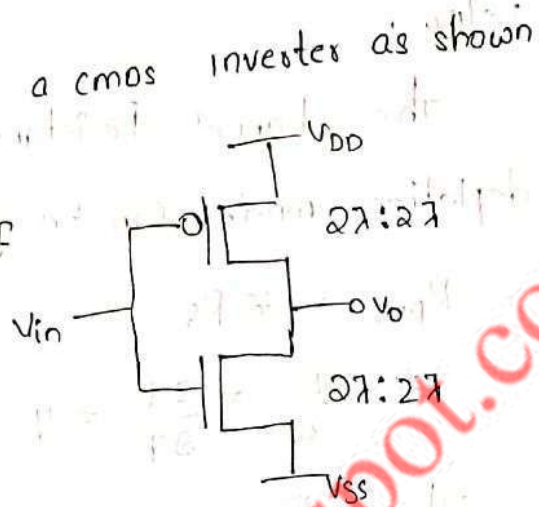
$$R_{pds} = 10 \text{ k}\Omega$$

$\therefore$ The on channel Resistance of CMOS inverter is

$$R_{on} = R_{pus} + R_{pds}$$

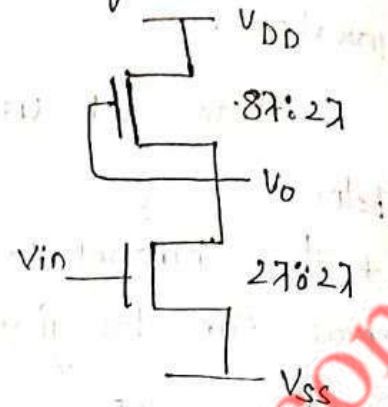
$$= 25 \text{ k}\Omega + 10 \text{ k}\Omega$$

$$= 35 \text{ k}\Omega$$



R_s values can be taken for 5μm technology for convenience.

The nmos Inverter is diagrammatically as shown below.



The channel Resistance of depletion mode can be given as

$$R_{pus} = Z \cdot R_s$$

$$Z = \frac{L}{W} = \frac{87}{27} = 4$$

$$\text{The } R_{pus} = 4 \cdot R_s$$

$$= 4 \cdot (2.5 \times 10^4)$$

$$= 40 \text{ k}\Omega$$

The channel Resistance of enhancement mode can be given as

$$R_{pds} = Z \cdot R_s$$

$$Z = \frac{L}{W} = \frac{27}{27} = 1$$

$$R_{pds} = 1 \cdot R_s$$

$$= 1(10^4)$$

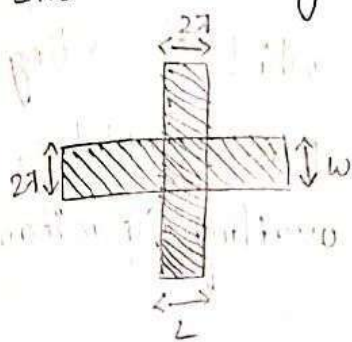
$$= 10 \text{ k}\Omega$$

The ON channel Resistance of nmos inverter can be is $R_{ON} = R_{pus} + R_{pds}$

$$= 40 \text{ k}\Omega + 10 \text{ k}\Omega$$

$$= 50 \text{ k}\Omega$$

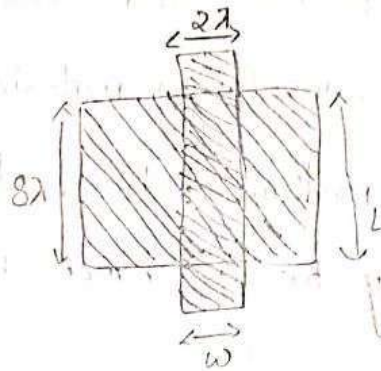
The sheet Resistance Concept can be extended for transistors, for example Consider two transistors as shown in figure 'a' and 'b' shown below.



$$L:W$$

$$2\lambda:2\lambda$$

figure 'a'



$$L:W$$

$$8\lambda:2\lambda$$

figure 'b'

In the above diagrams figure 'a' is having a length of '2λ' and a width of '2λ' and figure 'b' carries a length of '8λ' with a width of '2λ'.

for a fig 'a' the channel Resistance can be calculated as $R = Z R_s$

Where $Z = \frac{L}{W} = \frac{2\lambda}{2\lambda} = 1$

$$R = 1 \cdot R_s$$

$$R = 1 \cdot (10^4)$$

$$= 10K\Omega$$

the channel Resistance for fig 'b' can be calculated as $R = Z \cdot R_s$

$$Z = \frac{L}{W} = \frac{8\lambda}{2\lambda} = 4$$

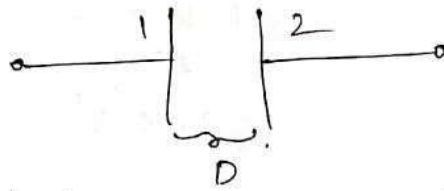
$$R = 4 \cdot R_s$$

$$= 4(10^4)$$

$$R = 40K\Omega$$

Area Capacitance of layers :-

In the IC fabrication process, the layers can be separated from one another by an oxide layer (i.e., insulating material) which is acting as a dielectric medium between two parallel plates, so there may be a chance of availing capacitance.



The Capacitance 'C' can be given as

$$C = \frac{\epsilon A}{D}$$

where ϵ = permittivity and can be given as

$$\epsilon = \epsilon_0 \epsilon_{ins}$$

$\epsilon_0 \rightarrow$ Absolute permittivity (or) permittivity of free space. (8.854×10^{-12} faraday/meter)

$\epsilon_{ins} \rightarrow$ Relative permittivity = 4 for silicon

A = Area of plates

D = thickness of SiO_2

* Some of the typical values of capacitance for 5 μm , 2 μm and 1.2 μm technologies can be tabulated below.

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Capacitance	Value in $\text{PF} \times 10^4 / \mu\text{m}^2$	Value in $\text{PF} \times 10^4 / \mu\text{m}^2$	Value in $\text{PF} \times 10^4 / \mu\text{m}^2$
	5 μm	2 μm	2 μm
gate to channel capacitance	4 (1.0)	8 (1.0)	16 (1.0)
diffusion (active)	1 (0.25)	1.75 (0.22)	3.75 (0.23)
polysilicon to substrate	0.4 (0.1)	0.6 (0.075)	0.6 (0.038)
Metal 1 to substrate	0.3 (0.075)	0.33 (0.04)	0.33 (0.02)
Metal 2 to substrate	0.2 (0.5)	0.17 (0.02)	0.17 (0.01)
Metal 2 to Metal 1	0.4 (0.1)	0.5 (0.06)	0.5 (0.03)
Metal 2 to polysilicon	0.3 (0.075)	0.3 (0.038)	0.3 (0.018)

Standard unit of Capacitance ($\square\text{Cg}$) :-

The standard unit of Capacitance can be define as gate to channel Capacitance of a MOS transistor having the feature size of $L=W$.

Here, for example standard unit of Capacitance can be calculated for different technologies.

For 5 μm technology :-

The area per standard square = $5\mu\text{m} \times 5\mu\text{m}$
 $= 25\mu\text{m}^2$

The standard unit of Capacitance ($\square\text{Cg}$) can be given as

$$\square\text{Cg} = \text{Area/standard square} \times \text{Capacitance}$$

$$\Rightarrow 25 \mu\text{m}^2 \times 4 \times 10^{-4} \text{ PF}/\mu\text{m}^2$$

$$\Rightarrow 100 \times 10^{-4} \text{ PF}$$

$$\square C_g = 0.01 \text{ PF}$$

for 2 μm technology

$$\text{Area/standard square} = 2 \mu\text{m} \times 2 \mu\text{m}$$

$$= 4 \mu\text{m}^2$$

The standard unit Capacitance ($\square C_g$) can be given as

$$\square C_g = \text{Area/standard square} \times \text{Capacitance}$$

$$= 4 \mu\text{m}^2 \times 8 \times 10^{-4} \text{ PF}/\mu\text{m}^2$$

$$= 32 \times 10^{-4} \text{ PF}$$

$$= 0.0032 \text{ PF}$$

for 1.2 μm technology

$$\text{Area/standard square} = 1.2 \mu\text{m} \times 1.2 \mu\text{m}$$

$$= 1.44 \mu\text{m}^2$$

The standard unit Capacitance ($\square C_g$) can be given as

$$\square C_g = \text{Area/standard square} \times \text{Capacitance}$$

$$= 1.44 \mu\text{m}^2 \times 16 \times 10^{-4} \text{ PF}/\mu\text{m}^2$$

$$= 23.04 \times 10^{-4} \text{ PF}$$

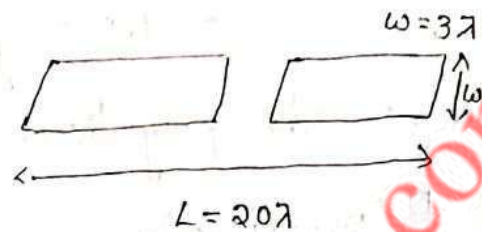
$$= 0.023 \text{ PF}$$

Some Area Capacitance Calculations:-

In this the relative values of Capacitance can be used for the representation of Capacitance and all values carried out in 'x' based values.

The Relative Area Can be represented as the ratio of Area of Interest to the standard Area.

$$\therefore \text{Relative Area} = \frac{\text{Area of interest}}{\text{standard Area}}$$



$$\begin{aligned} \text{Relative Area} &= \frac{207 \times 37}{27 \times 27} \\ &= \frac{607^2}{47^2} = 15 \end{aligned}$$

(*) for 5um technology

(i) The Capacitance to Substrate Can be given as

$\Rightarrow$ Relative area $\times$ Capacitance

$$= 15 \times 0.075 \square \text{cg}$$

$$= 1.125 \square \text{cg}$$

$\therefore$ The Capacitance to substrate is 1.125 $\square \text{cg}$ times of Square $\text{cg} (\square \text{cg})$.

(2) The diffusion Capacitance Can be calculated

as $=$ Relative area $\times$ Capacitance

$$= 15 \times 0.25 \square \text{cg}$$

$$= 3.75 \square \text{cg}$$

$\therefore$ The diffusion Capacitance is 3.75 times of $\square \text{cg}$.

3) For polysilicon

The Capacitance for polysilicon can be calculated as = Relative Area $\times$ Capacitance.

$$= 15 \times 0.1 \text{ } \square\text{Cg}$$

$$= 1.5 \text{ } \square\text{Cg}$$

$\therefore$ The polysilicon Capacitance is 1.5 times of $\square\text{Cg}$

Delay unit (τ):-

The delay unit (τ) can be given as the product of Sheet Resistance (R_s) and standard unit of gate Capacitance ($\square\text{Cg}$).

$$\tau = R_s \square\text{Cg}$$

for 5 μm technology

$$\text{WKT } \tau = R_s \square\text{Cg}$$

$$= 10^4 \times 0.01 \text{ PF}$$

$$= 10^4 \times 0.01 \times 10^{-12}$$

$$= 100 \times 10^{-12}$$

$$= 1 \times 10^{-10}$$

$$= 0.1 \times 10^{-9}$$

$$\tau = 0.1 \text{ nsec}$$

for 2 μm technology

$$\text{WKT } \tau = R_s \square\text{Cg}$$

$$= 2 \times 10^4 \times 32 \times 10^{-4} \text{ pf}$$

$$= 64 \text{ pf}$$

$$\tau = 0.034 \text{ nsec}$$

for 1.2 μm technology

$$\tau = R_s C_g$$

$$= 2 \times 10^4 \times 23.04 \times 10^9 \text{ pF}$$

$$= 46.08 \times 10^{-13}$$

$$\tau = 0.046 \text{ nsec}$$

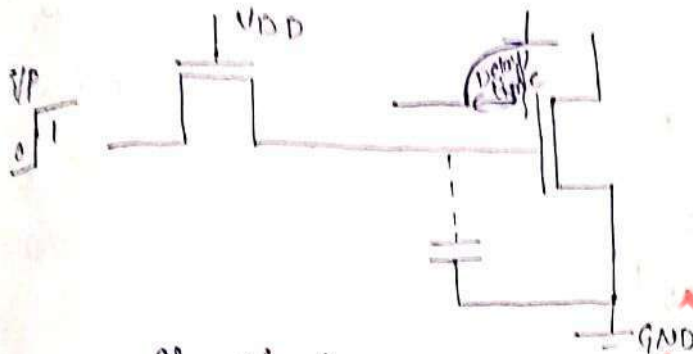


fig: Simple model to calculate delay time.

We know that the electron transit time τ_{ds} as

$$\tau_{ds} = \frac{L^2}{\mu v_{ds}}$$

* When i/p signal is transmitted through the pass transistors the output voltage will get reduce to 63% of V_{DD} that is $0.63 \times V_{DD}$

$$= 0.63 \times 5 \text{ V}$$

* for 5 μm technology

$$\tau_{ds} = \frac{L^2}{\mu v_{ds}}$$

$$= \frac{5 \mu\text{m} \times 5 \mu\text{m}}{650 \text{ cm}^2/\text{V-sec} \times 3 \text{ V}}$$

$$\begin{aligned}
 &= \frac{25(10^{-6})^2 \text{ m}^2}{650(0.01) \sqrt{\text{sec}} \times 3\sqrt{V}} \\
 &= \frac{25 \times 10^{-12}}{650 \times 0.01 \times 3} \text{ sec} \\
 &= \frac{25 \times 10^{-12}}{19.5} \\
 &= \frac{25 \times 10^{-3} \times 10^{-9}}{19.5} \\
 &= \frac{2.5 \times 10^{-9}}{19.5 \times 10^3} \\
 &= 0.128 \times 10^{-9} \\
 &\approx 0.13 \text{ nsec}
 \end{aligned}$$

Note:- The delay unit τ_1 is approximately equal to the electron transit time τ_{ds} .

Inverter Delay:-

nmos Inverter Delay:-

Here let us consider an nmos inverter with a ratio of 4:1.

The pull up to pulldown ratio of nmos driven by another nmos is 4:1.

$$\text{i.e., } \frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$$

$$Z_{pu} = 4 Z_{pd}$$

$$Z_{pu} = 4 R_s$$

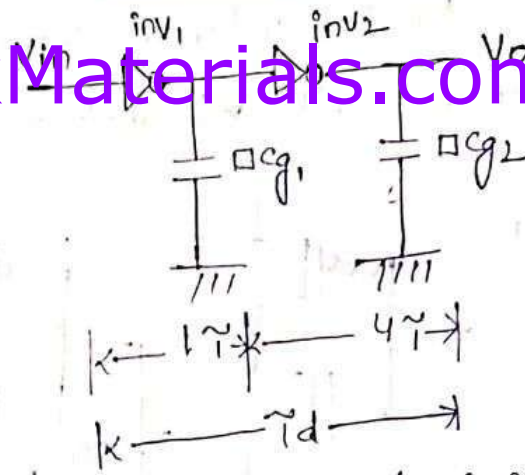
$$\frac{R_{pu}}{R_{pd}} = \frac{4}{1}$$

$$R_{pu} = 4 R_{pd}$$

$$R_{pu} = 4 R_s$$

$$R_{pu} = 4 \times 10^4$$

$$R_{pu} = 40 k\Omega$$



* The delay is not effected by the Cascade connections of inverters but it is due to the turning on/off actions

* The total delay τ_d is the combination of both inverters.

$$\text{i.e, } \tau_d = 1\tau + 4\tau$$

$$= \tau[1+4]$$

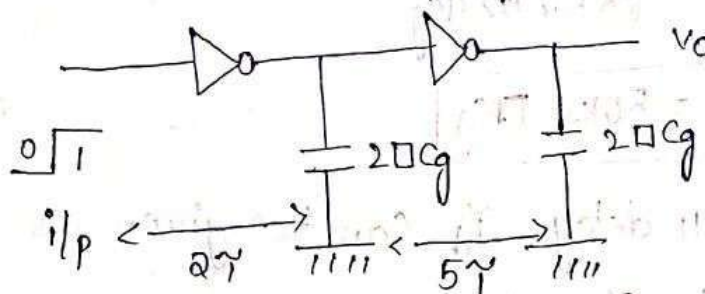
$$= \tau[1+\frac{4}{1}]$$

$$\tau_d = \tau \left[1 + \frac{Z_{pu}}{Z_{pd}} \right]$$

$\therefore$ The total delay for an nmos inverter is $\tau_d = 5\tau$.

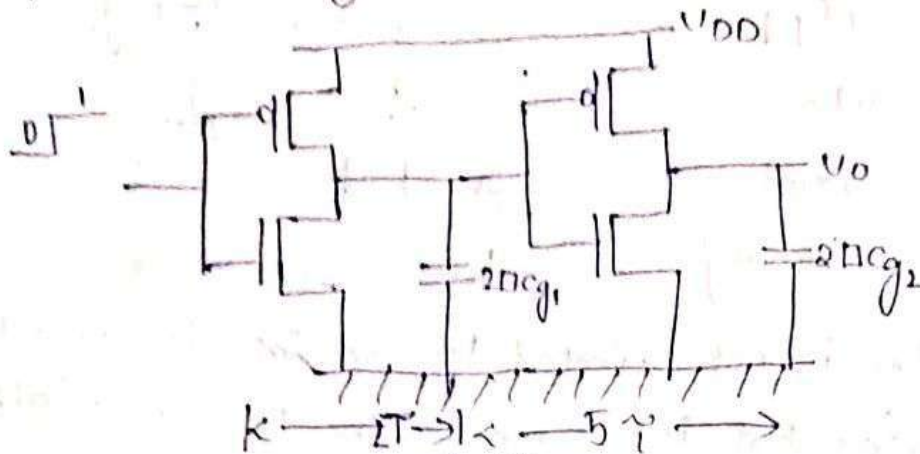
CMOS Inverter Delay:-

Here let us Consider an arrangement shown below for the Calculation of CMOS inverter delay.



fig(a)

Due to the internal wiring capacitance the load capacitance will get doubled that is $2C_g$



fig(b):

* When i/p is V_{DD} (logic 1). then the nmos of inverter will get on and the Capacitor will get discharge path through the nmos.

i.e., $\tau_1 = R_n 2C_g$

$$\tau_1 = 20k\Omega \cdot C_g$$

* When the capacitor of inverter 1 is discharge then at the input of inverter 2 we have logic '0'. i.e., pmos of inverter 2 will get on and the capacitor will get charge.

i.e., $\tau_2 = R_p 2C_g$
 $= (25k\Omega) \times 2C_g$

$$\tau_2 = 50k\Omega \cdot C_g$$

$\therefore$ The overall delay τ_d can be given as

$$\tau_d = \tau_1 + \tau_2$$

$$= 20k\Omega \cdot C_g + 50k\Omega \cdot C_g$$

$$= 2R_s \square C_g + 5R_s \square C_g$$

$$= R_s \square C_g (2+5)$$

$$\tau_d = 7\tau$$

∴ The overall delay of CMOS inverter is 7τ .

* The overall delay can be better understood with a calculations of Rise time (τ_r) and fall time (τ_f).

Rise time Calculation (τ_r):-

The calculation of Rise time ' τ_r ' can be done when input is logic '0'.

WKT I_{ds} for saturation

$$I_{ds} = \frac{K_n}{2} [V_{gs} - V_{t_n}]^2$$

$$I_{ds} = \frac{\beta_p}{2} [V_{gs} - V_{t_p}]^2 \rightarrow (1)$$

$$V_{out} = I_{ds} R \rightarrow (2)$$

$$\text{WKT } \tau_r = RC_L$$

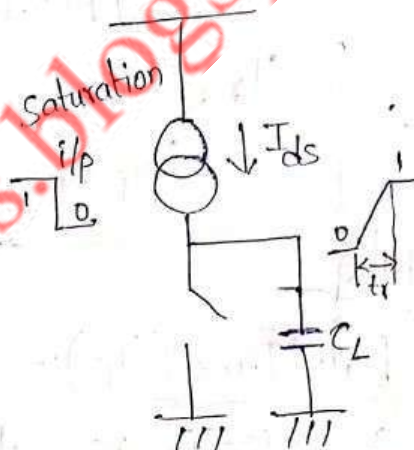
$$R = \frac{\tau_r}{C_L} \rightarrow (3)$$

Sub (3) in (2)

$$V_{out} = I_{ds} \cdot \frac{\tau_r}{C_L}$$

$$\tau_r = \frac{V_{out} C_L}{I_{ds}}$$

$$= \frac{V_{out} C_L}{\frac{\beta_p [V_{gs} - V_{t_p}]^2}{2}}$$



$$\tau_r = \frac{2 V_{out} C_L}{\beta_P [V_{GS} - |V_{tp}|]^2}$$

$$V_{GS} = V_{DD}$$

$$V_{out} = V_{DD}$$

$$V_{tp} = 0.2 V_{DD}$$

$$\tau_r = \frac{2 \cdot V_{DD} C_L}{\beta_P [V_{DD} - 0.2 V_{DD}]^2}$$

$$\tau_r = \frac{2 V_{DD} C_L}{\beta_P [0.8 V_{DD}]^2}$$

$$= \frac{2 V_{DD} C_L}{\beta_P (0.64) V_{DD}^2}$$

$$= \frac{2 C_L}{\beta_P (0.64) V_{DD}}$$

$$\tau_r \approx \frac{3 C_L}{\beta_P V_{DD}}$$

7.1.1.2

Fall Time (T_f):- The Fall time (T_f) can be calculated Similarly to Rise time (T_r) Calculation.

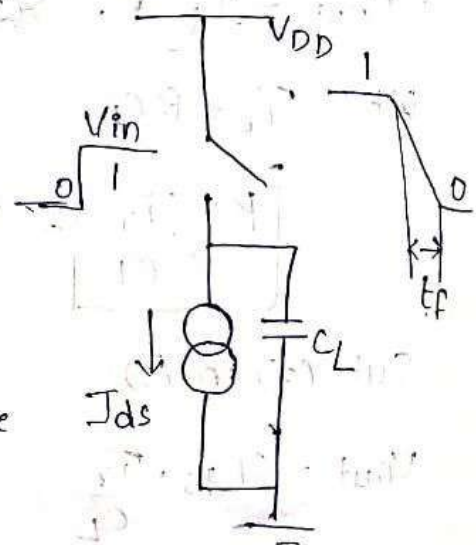
* The fall time T_f can be given as

$$T_f = \frac{3 C_L}{\beta_n V_{DD}}$$

(reference from Rise time Calculation)

* The ratio of Rise time to fall time can be given as

$$\frac{T_r}{T_f} = \frac{\frac{3 C_L}{\beta_P / V_{DD}}}{\frac{3 C_L}{\beta_n / V_{DD}}}$$



$$\therefore T_r \propto \frac{1}{\beta_p} \quad \text{and fall Time } T_f \propto \frac{1}{\beta_n}$$

* The rise time ' T_r ' and fall time ' T_f ' both are $\propto CL$ and $\propto \frac{1}{V_{DD}}$.

Driving large Capacitive loads:-

* The concept of driving large capacitive loads may arise when the signals are propagating from on-chip to off-chip peripherals, which are having comparatively very large values.

* Here the load capacitance ' C_L ' is equal orders > than the gate capacitance ' C_g ' i.e.,

$$C_L > 10^4 C_g \text{ [Assumption].}$$

* In order to have decreased delay we need to maintain increased channel length which may further decrease the resistance.

* To drive large capacitive loads we are having 3 techniques.

1. Cascoded Connections of Inverters as drivers.

2. Superbuffers as drivers.

3. Bi-CMOS drivers.

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1. Cascaded Connections of Inverter as drivers:-

* When driving large capacitive loads to have a minimum delay we should have low resistances.

* Low resistances can be obtained by having low Z_{pu} & Z_{pd} 's

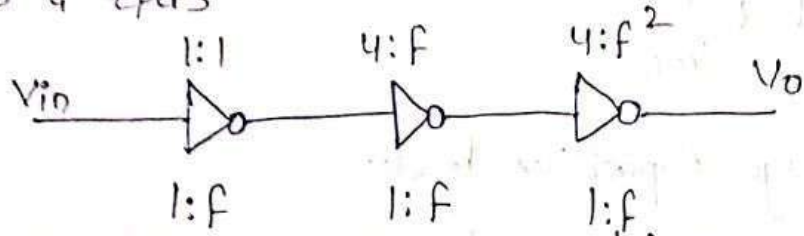


fig:- Cascaded inv as drivers

* The arrangement of Cascaded inverters as drivers is shown below.

* If we increase the width factor 'f' then the load on capacitance may increase that results in larger capacitive area.

* If there is increase in width factor then the resistance will get automatically decrease thereby we can have minimum delay.

for nmos:- Delay/stage = $1f\gamma$ for ΔV_{in}
 $= 4f\gamma$ for ∇V_{in}

$$\tilde{\tau}_d = 1f\gamma + 4f\gamma = 5f\gamma$$

for pmos:- Delay/stage = $2f\gamma$ for ΔV_{in}
 $= 5f\gamma$ for ∇V_{in}

$$\tilde{\tau}_d = 2f\gamma + 5f\gamma = 7f\gamma$$

* The relation b/w no. of inverters 'N' to width factor 'f' can be given as

$$N^f = \frac{C_L}{C_g} = y$$

$$N^f = y$$

Apply 'log' on both sides

$$f \log N = y$$

* If $f = e$, $e \log N = y$

$$N \log e = y$$

$$N = y$$

* If $N = \text{even}$, then the delay is

$$\tau = \frac{N}{2} \quad 5f\tau = 2.5f\tau \text{ for nmos}$$

$$\tau = \frac{N}{2} \quad 7f\tau = 3.5f\tau \text{ for cmos}$$

* If $N = \text{odd}$, then the delay is

$$\tau = [2.5(N-1) + 4]f\tau \text{ for nmos} \quad \Delta V_{in}$$

$$\tau = [3.5(N-1) + 5]f\tau \text{ for cmos} \quad \Delta V_{in}$$

$$\tau = [2.5(N-1) + 1]f\tau \text{ for nmos} \quad \Delta V_{in}$$

$$\tau = [3.5(N-1) + 2]f\tau \text{ for cmos} \quad \Delta V_{in}$$

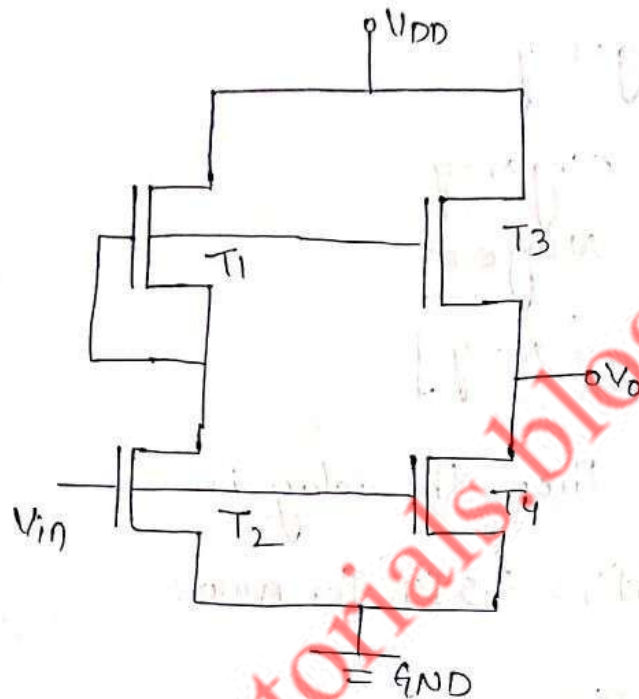
Note:- If there is increasing width factor 'f' then no. of transistors per chip will get reduced.

2. Super buffers or drivers:- It is classified into two types.

1. Inverting type super buffers

2. Non inverting type super buffers

1. Inverting type Superbuffers:-



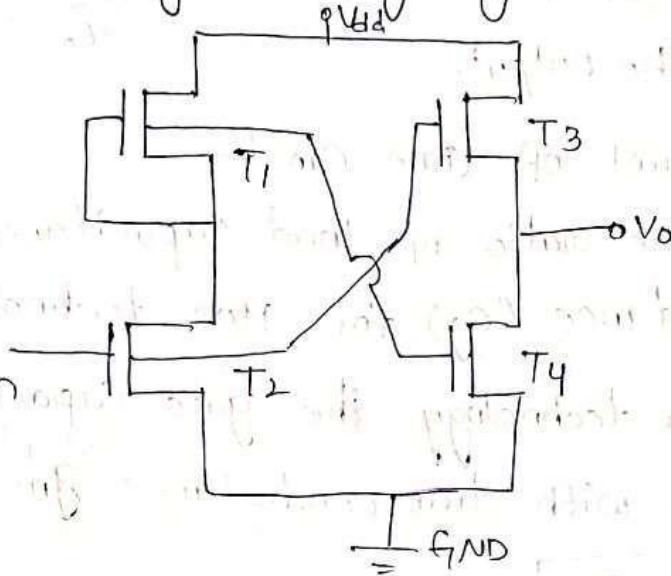
* When V_{in} is logic '0' then the transistors T_2 & T_4 will get off and the transistors T_1 & T_3 will get on, thereby producing o/p as logic '1'.

* If V_{in} is logic '1' then the transistors T_1 & T_3 will get on and the transistors T_2 & T_4 will get off thereby producing o/p as logic '0'.

2. Non-inverting type Super buffers:-

* When V_{in} is logic '0' then the transistors T_1 & T_4 will get on and the transistors T_2 & T_3 will get off thereby producing o/p as logic '0'.

* when V_{in} is logic '1' then the transistors T_2 & T_3 will get on and the transistors T_1 & T_4 will get off and thereby producing logic '1'.



21/1/19

Bipolar Drivers:-

1. In Bipolar technology, the output drive current is more for a given minimum silicon area.

2. In this the transconductance g_m and low current driving capabilities and current/area (or) more compared to MOS technology.

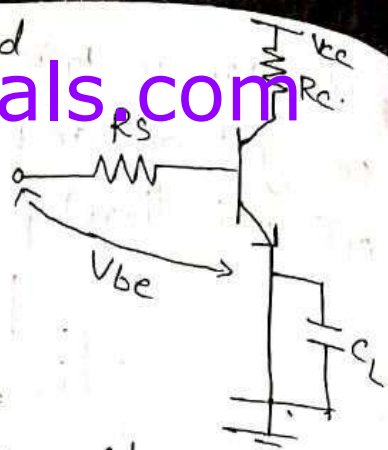
* In this the current I_c is exponentially related to the input voltage.

* In this technology it is having the capability of driving large currents for the application of smaller voltages. and the current through the device depends on the base width w_b and the amount of doping level.

A simple representation that is use bipolar technology to change their states is shown below.

* The amount of time required to change the input is equal

to amount of time taken to change the output.



* The amount of time can be given as the ratio of load capacitance (C_L) to gate capacitance (C_g) for MOS technology $\Delta t = \frac{C_L}{C_g}$

* In Bipolar technology the gate capacitance C_g is replaced with transconductance g_m .

$$\Delta t = \frac{C_L}{g_m}$$

* Therefore the total time taken can be represented as follows

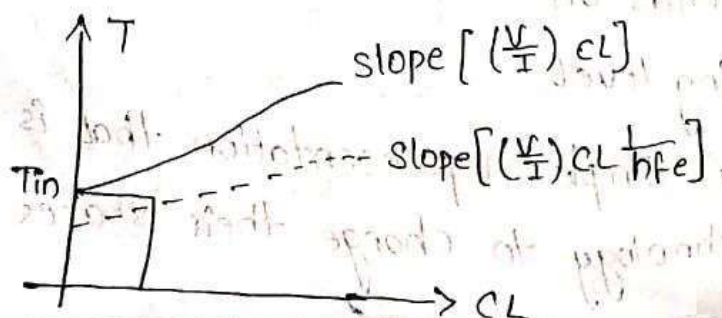
$$T = T_{in} + \left(\frac{V}{I} \right) C_L \frac{1}{h_{fe}} \quad \text{for bipolar}$$

Where T_{in} - the inbuilt time produced by device

C_L - load capacitance

h_{fe} - Current amplification factor.

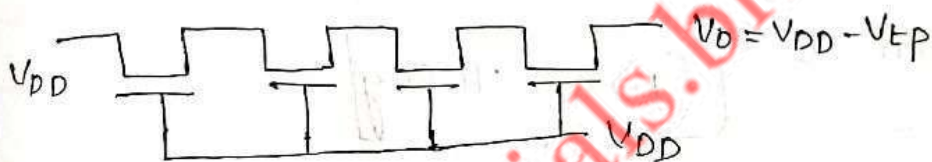
The graphical representation of MOS and bipolar technology are drawn as below:



propagation delays:-

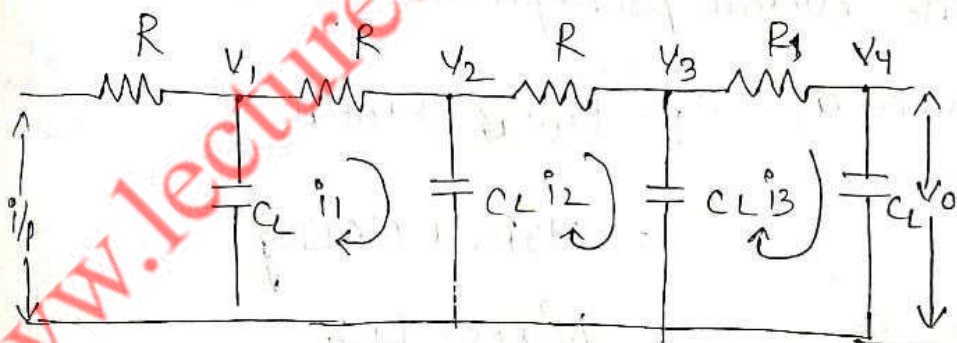
To transfer logic levels from one place to another place we are using series of pass transistors in b/w two points:-

Here in this case nmos pass transistors are use in series connection, all the gate terminals are tight together and it is being given V_{DD} .
for example a series of four pass transistors are shown below.



Model for propagation delay

The equivalent circuit model can be drawn as



At node 2, we get write $C \frac{dv_2}{dt} = i_1 - i_2$

$$C \frac{dv_2}{dt} = \frac{V_1 - V_2}{R} - \frac{V_2 - V_3}{R}$$

$$C \frac{dv_2}{dt} = \frac{V_1 - 2V_2 + V_3}{R}$$

$$RC \frac{dv_2}{dt} = V_1 - 2V_2 + V_3$$

$$R \frac{dv}{dt} = \frac{d^2x}{dx^2}$$

$\therefore x \Rightarrow$ distance

$\therefore$ The propagation delay $t_p \propto x^2$.

* For 'N' no of networks the total resistance

Can be given as $R_{total} = N \times R_s$

Where R_s - sheet Resistance

γ - relative Resistance

N - no. of stages

* For 'C' the total no of capacitance can be given as

$$C_{total} = N \times C \square C_g$$

Where C -

* The overall propagation delay t_p can be

given as $t_p = R_{total} \times C_{total}$

$$= N \times R_s \times N \times C \square C_g$$

$$= N^2 \times R_s \times C \square C_g$$

$$= N^2 \times \gamma \times R_s \square C_g$$

$$t_p = N^2 \gamma \tau$$

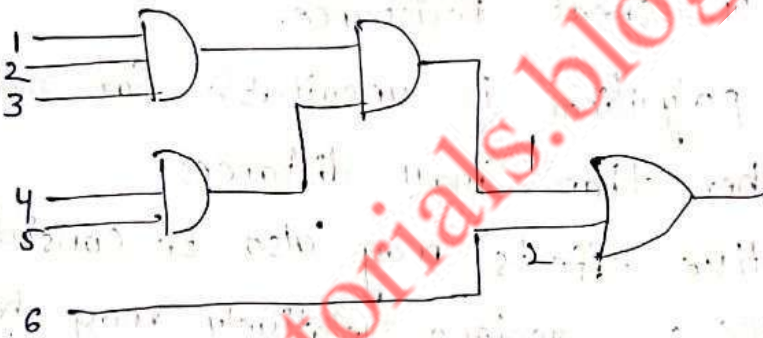
$$\tau = R_s \square C_g$$

If there is increase in N , it results in increased propagation delay.

fan-in and fan-out characteristics:-

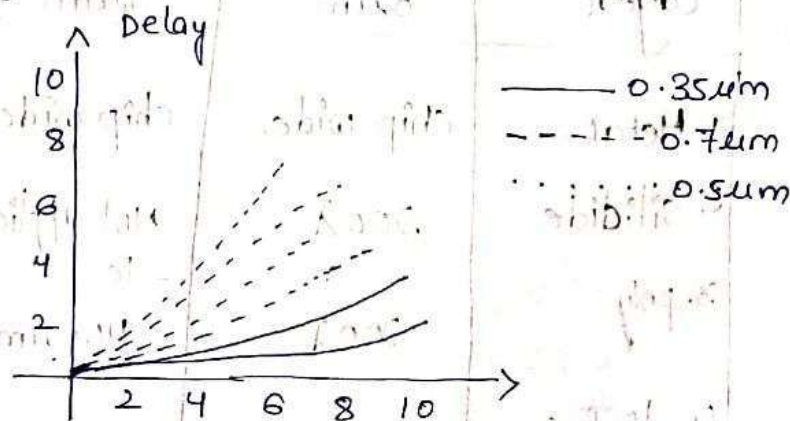
We have two major factor that influence operational speed of a gate terminal these are fan-in and fan-out.

fan-in:- The maximum no. of inputs that are applied to driven in gate is called fan-in



Fan-out:- The max no. of i/p's that are applied to driven gate is called fan-out.

* The delay associated with Fan-in & Fan-out for three technologies is represented as



Fan-in & fan-out characteristics

In designing circuits for our convenience of suitable specifications we have to consider several number of considerations which includes choice of layers

1. V_{DD} and V_{SS} should be distributed on metal layer whenever possible.
2. The length of polysilicon should be used after careful consideration because of relatively high value of sheet resistance.
3. The polysilicon is unsuitable for routing V_{DD} & V_{SS} other than small distances.
4. Capacitive effects may also be considered because the diffusion regions relatively may have high capacitive values to the substrate.

Table for electrical rules:-

Layers	Max length of wires		
	5 μ m	2 μ m	1.2 μ m
1. Metal	chip wide	chip wide	chip wide
2. Silicide	200 λ	Not applicable	Not applicable
3. poly	200 λ	400 μ m	250 μ m
4. diffusion	20 λ	100 μ m	60 μ m

layer	capacitance	Resistance	comment
1. Metal	Low	Low	* Good current capability without large voltage drop and it is used for power distributions and global.
2. silicide	Moderate	Moderate	* It has RC product has a moderate value, long wires are applicable: this layer is useful in place of poly silicon in some cases of nmos process
3. poly silicon	Moderate	High	* It has RC product has IR moderate and high drop
4. diffusion (Active)	High	Moderate	* RC product is moderate and it has moderate IR drop hence it is hard to drive

We have Area Capacitance contributed in the Calculation, pf. overall Calculation Capacitance.

The Area Capacitances are associated with the layers to substrate and from gate to channel.

We have three other Source for the Calculation of overall Capacitance.

1. Inter layer Capacitance

2. peripheral (Junction) Capacitance

3. (fringing field) fringing fields capacitance

1. Inter layer Capacitance:-

parallel plate effects are present b/w one layer to another layer.

for example, for a given area metal to polysilicon capacitance is higher than metal to substrate capacitance.

2. peripheral Capacitance:-

The source and drains of n-diffusion regions forms junctions with p-type substrate at uniform depth.

Similarly, p-active regions may form junctions with n-well (or) n type of substrate.

* for diffusion regions each diode thus form has associated with peripheral capacitance which is measured in PF/unit length.

The typical values for different technologies given by

diffusion Capacitance	Chemical Values		
	5 μ m	2 μ m	1.2 μ m
1. C_{Area}	1.082×10^{-4} PF/ μ m ²	1.25×10^{-4} PF/ μ m ²	1.7×10^{-4} PF/ μ m ²
2. $C_{peripheral}$	8×10^{-4} PF/ μ m	negligible	negligible

3. fringing fields:-

Capacitance due to fringing field effect can be a major component of overall capacitance of inter connected wires.

fringing field Capacitance can be of same order of area capacitance.

The capacitance of fringing field can be given as

$$C_{ff} = \epsilon_{ins} \epsilon_0 l \left[\frac{\pi}{\ln \left\{ 1 + \frac{2d}{t} \left(1 + \sqrt{\frac{t}{d}} \right) \right\}} - \frac{t}{4d} \right]$$

where l = length of the wire

t = thickness of the wire

d = Separation b/w wire and substrate.

* The total wire capacitance can be given as

$$C_w = C_{\text{Area}} + C_{ff}$$

Where C_{Area} = Area Capacitance

C_{ff} = fringing field Capacitance

Micro electronic technology can be characterised with the help of several indicators (or) figure of merits which includes

1. No of transistors per chip
2. minimum feature size
3. power dissipation
4. max operational frequency
5. die size
6. production cost

* many of these fig of merits can be improved by reducing dimensions of transistors, interconnections and separation b/w features and by adjusting doping level and supply voltage.

Scaling Models and Scaling factors:-

Basically we are having two scaling models

1. Constant electric field scaling model
2. constant voltage scaling model

In accordance with these two scaling models we are having a special scaling model which is the combination of both scaling models stated above and is called as combined voltage above and dimension scaling model.

The following fig indicates that substrate doping level which are associated with scaling of transistors.

* To scale any parameter we are using two scaling factors as $\frac{1}{\alpha}$ & $\frac{1}{\beta}$

* $\frac{1}{\beta}$ is used for supply voltage levels (V_{dd}) and for gate oxide thickness (t_o) for all other linear dimensions we use $\frac{1}{\alpha}$ as a scaling factor for both horizontal and vertical dimensions.

Note:- For Constant electric field scaling model we use $\beta = \alpha$ and for Constant voltage scaling model $\beta = 1$.

Scaling factors for device parameters:-

1. Gate area (A_g):- $A_g = L \times W$

'L' is the length of the channel which is scaled by $\frac{1}{\alpha}$

and 'w' is the width of channel which is scaled by $1/\alpha$

$$A_g = L \times w$$

$$= \frac{1}{\alpha} \times \frac{1}{\alpha}$$

$$A_g = \left(\frac{1}{\alpha^2}\right)$$

2. Gate Capacitance per unit area (C_o or C_{ox}):-

$$C_x = \frac{\epsilon}{D}$$

where ϵ = permittivity

D = gate oxide thickness

$$C_x = \frac{\epsilon}{D} = \frac{\epsilon_0 \epsilon_{ins}}{D} = \frac{1}{1/\beta} = \beta$$

3. Gate Capacitance (C_g):- $C_g = C_o w L$

where $C_o \Rightarrow$ absolute capacitance and it is scaled by β .

$$C_g = C_o w L = \beta w L = \beta \left(\frac{1}{\alpha}\right) \left(\frac{1}{\alpha}\right)$$

$$= \frac{\beta}{\alpha^2}$$

4. parasite capacitance (C_x):-

$$C_x = \frac{A_x}{d}$$

A_x = Area, d = separation

$$C_x = \frac{1/\alpha^2}{1/\alpha} = 1/\alpha$$

5. Carrier density in the channel (Q_{on}):-

$$C = \frac{Q}{V}$$

$$C_o V_{gs} = Q_{on}$$

6. channel on Resistance:-

$$R_{on} = \frac{L}{\omega} = \frac{1/d}{1/d} = 1$$

7. gate delay (T_d):-

$$\begin{aligned} T_d &= R_{on} G \\ &= 1 \cdot \beta/d^2 \\ &= \beta/d^2 \end{aligned}$$

8. Maximum operating frequency (f_o):-

$$\begin{aligned} f_o &= \frac{\omega}{L} \frac{\mu C_o V_{dd}}{C_g} = \frac{\beta \cdot \frac{1}{\beta}}{\beta/d^2} = \frac{1}{\beta/d^2} \\ &= \frac{d^2}{\beta} \end{aligned}$$

9. Saturation Current (I_{ds}):-

$$\begin{aligned} I_{ds} &= \frac{K\omega}{L} \frac{[V_{gs} - V_t]^2}{2} \\ &= \frac{1}{2} \left[\frac{1}{\beta} - \frac{1}{\beta} \right] L \\ &= \frac{1}{\beta^2} \end{aligned}$$

$$\begin{aligned} I_{ds} &= \frac{C_o \omega \mu}{L} \frac{[V_{gs} - V_t]^2}{2} \\ &= \beta \cdot \frac{1}{\beta^2} \\ &= \frac{1}{\beta} \end{aligned}$$

10. Current density (J):-

$$J = \frac{I_{ds}}{A} = \frac{1/\beta}{1/d^2} \\ = d^2/\beta$$

11. Switching energy per gate:-

$$E_g = \frac{1}{2} C_g V_{dd}^2 \\ = \frac{1}{2} \frac{\beta}{d^2} \cdot \frac{1}{\beta^2} \\ = \frac{1}{2d^2\beta}$$

12. power dissipation per gate:-

$$P_g = P_{gs} + P_{gd} \quad P_{gs} = \frac{V_{dd}^2}{R_{on}}, \quad P_{gd} = E_g \cdot f_0$$

$$P_{gs} = \frac{1/\beta^2}{1} = 1/\beta^2, \quad P_{gd} = 1/\beta^2$$

$$P_g = 2/\beta^2 = 1/\beta^2$$

13. power dissipation per unit area (P_A):-

$$P_A = \frac{P_g}{\text{Area}} = \frac{1/\beta^2}{1/d^2} \\ = d^2/\beta^2$$

14. power speed product:-

$$P_t = P_g T_d = 1/\beta^2 \cdot \beta/d^2 \\ = 1/d^2\beta$$

S.No	parameter	Combined Voltage and dimension model	Constant electric field model $\beta = \alpha$	Constant Voltage Scaling model $\beta = 1$
1.	Supply Voltage (V_{dd})	$1/\beta$	$1/\alpha$	1
2.	Channel length (L)	$1/\alpha$	$1/\alpha$	$1/\alpha$
3.	width of the channel (w)	$1/\alpha$	$1/\alpha$	$1/\alpha$
4.	gate oxide thickness (D)	$1/\beta$	$1/\alpha$	1
5.	gate Area (A_g)	$1/\alpha^2$	$\frac{1}{\alpha^2}$	$\frac{1}{\alpha^2}$
6.	gate capacitance per unit area (C_D)	β	α	1
7.	gate capacitance (C_g)	β/α^2	$\frac{\alpha}{\alpha^2} = \frac{1}{\alpha}$	$\frac{1}{\alpha^2}$
8.	parasitic Capacitance	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$
9.	Carrier density in the channel (Q_{on})	1	1	1
10.	Channel on Resistance	1	1	1
11.	gate delay	β/α^2	$1/\alpha$	$1/\alpha^2$
12.	maximum operating frequency	α^2/β	α	α^2

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13.	Saturation Current density	$1/\beta$	$1/d$	1
14.	Switching energy per gate	α^2/β	α	α^2
15.	power dissipation per gate	$1/\alpha^2\beta$	$1/\alpha^3$	$1/\alpha^2$
16.	power dissipation per unit area	$1/\beta^2$	$1/\alpha^2$	1
17.	power speed product	α^2/β^2	1	α^2
18.	power speed product	$1/\alpha^2\beta$	$1/\alpha^3$	$1/\alpha^2$

Limitations of Scaling:-

Substrate Doping:-

So far we are discussed about various effects, we have neglected built in (junction) potential V_B which intuned depends on substrate doping level and this is acceptable so long as V_B is smaller compared to V_{DD} .

Substrate doping Scaling factors:-

As the length of the channel of a mos transistor is reduce, that depletion region width also to be scaled down to prevent a source and drain depletion regions from meeting.

The depletion width 'd' for the junction can be given as

$$d = \sqrt{\frac{2\epsilon_0\epsilon_{ins} V_B}{qN_B}}$$

Where $q = \text{charge}$
 $\epsilon_0 = \text{permittivity of free space}$
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$\epsilon_{ins} = \text{permittivity of material}$

$V_B = V_{\text{built in potential}}$

The inbuilt potential V_B can be given as

$$V_B = \frac{kT}{q} \ln \left[\frac{N_D N_B}{n_i^2} \right]$$

Where $N_D = \text{drain (or) Source doping level}$

$n_i = \text{intrinsic Carrier Concentration}$

* If we increase N_B to reduce d , at the same time V_B is also increase.

* For Combined Voltage & dimension model the total applied voltage can be given as

$$V_a = m V_B$$

Where m is a real number

$$\text{then } V = V_a + V_B$$

$$V = m V_B + V_B$$

$$V = V_B (m+1)$$

Now if is scale down V_a then the voltage can be given as

$$V_a = \frac{m V_B}{\beta}$$

$$V = \frac{m V_B}{\beta} + V_B$$

$$V_2 = \frac{V_B(m+\beta)}{\beta}$$

∴ The effective Scale voltage can be given as

$$V_S = \frac{V_2}{V_1} = \frac{V_B(m+\beta)}{\beta V_B(m+1)}$$

$$V_S = \frac{(m+\beta)}{\beta(m+1)}$$

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Limitations due to Sub threshold Currents (I_{sub}):-

one of the major concern in the scaling of devices is the effect of Sub threshold Current I_{sub} which can be given as

$$I_{sub} \propto e^{\frac{(V_{GS}-V_T)}{K T/q}}$$

When a transistor is in off state, the value of $V_{GS}-V_T$ is negative and it should be as large as possible to minimize I_{sub} .

As the voltages are scaled down then the ratio of $V_{GS}-V_T$ to $K T/q$ will reduce so that Sub threshold increase.

* For this reason, it may be desirable to scale both v_{gs} & v_t by a factor $1/b > 1/a$. Since a is generally greater than b .

* The maximum electric field across the depletion region can be given as

$$E_{max} = \frac{2V}{d} = \frac{2(V_a - V_b)}{d}$$

* The junction breakdown Voltage can be given as

$$BV = \frac{\epsilon_0 \epsilon_{ns} E^2}{2qNB}$$

Note- Extra care is therefore require in estimating the breakdown voltages for scaled devices.

* The Electric field are greater and breakdown Voltage is greater at the corner of diffusion regions underlying SiO_2 .

Limitations on logic levels and Supply Voltages due to noise:-

The major advantages in scaling of devices are smaller gate delay time i.e. higher operating frequency and lower internal power consumption.

* The lowering of interface spacing and higher switching increase noise in VLSI chips. so noise may also be amplified and is thus a major concern.

* The mean square current fluctuations in the channel can be given as

$$i^2 = 4kT R_{ngm} \Delta f \rightarrow (1)$$

where R_n = noise Resistance

Δf = Band width

g_m = BV_p

V_p = pinch off Voltage

The equivalent Resistance R_n can be given as

$$R_n = \left(\frac{1}{2} \frac{V_g}{V_p} + \frac{1}{6} \right) \frac{1}{g_m} \rightarrow (2)$$

where $V_g = V_{gs} - V_t + V_B$

$V_p' = V_p + V_B$

Similarly the thermal equivalent ' R_{ngm} ' can be given as

$$R_{ngm} = \frac{1}{2} \frac{(V_{gs} - V_t + V_B)}{(V_p + V_B)} + \frac{1}{6} \rightarrow (3)$$

Observing eqn(3) the value ' R_{ngm} ' is also dependent on V_g but very small extent. for

The modified expression for R_{ngm} when t_{ox} is scaled as

$$R_{ngm}^{tox} = \frac{1}{2} \left[\frac{V_g}{V_g - \frac{1}{2} \left(\frac{a}{C_{ox}} \right)^2 \left(1 + \frac{V_p'}{a} \right)^{1/2} - 1} \right] + \frac{1}{6}$$

* If there is an increase in the value of C_{ox} then R_{ngm} decreases by a small amount which in turn decrease the ratio of logic levels to thermal noise by same amount.

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Switch logic:-

Switch logic is based on pass transistors (or) on the transmission gates.

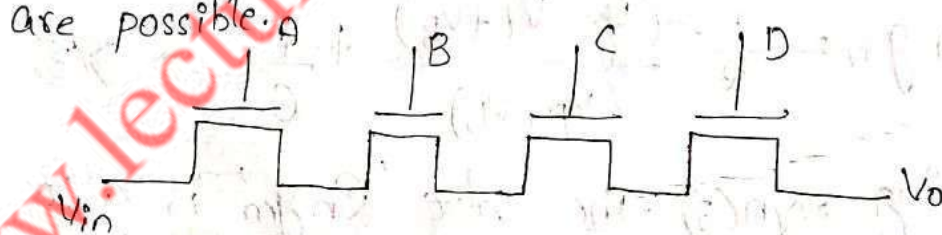
* This approach is fast for small arrays and takes no static current from supply rails.

* Hence power dissipation such arrays is small.

∴ Current flow only on switching.

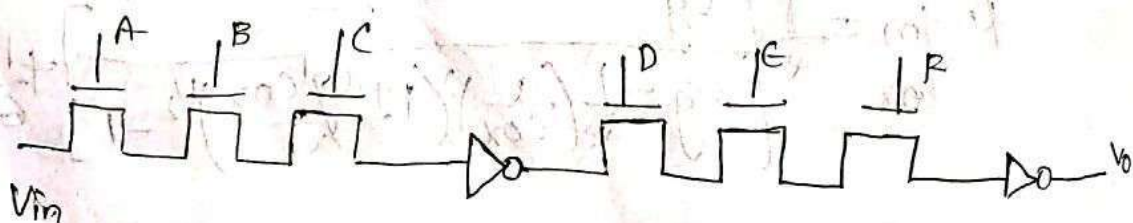
* pass transistor logic is similar to logic arrays based on delayed contacts.

* The basic AND connections are set out as shown in fig below but many combinations of switches are possible.

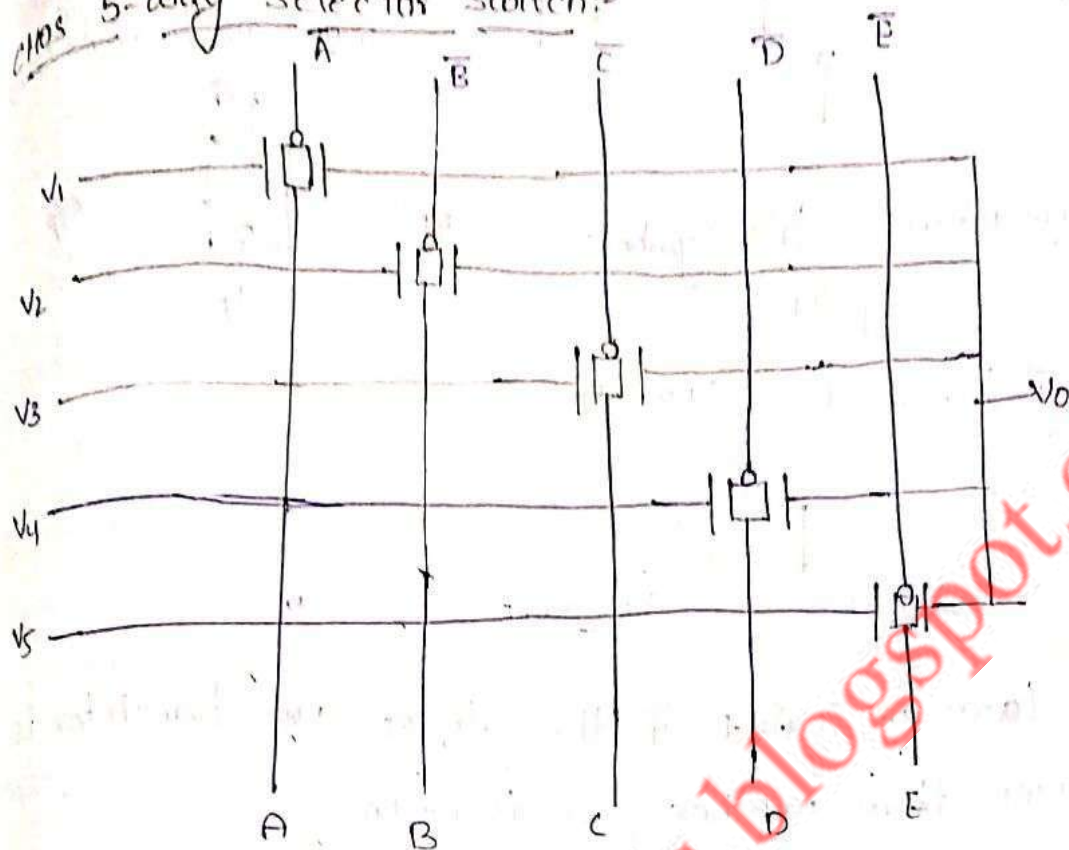


$V_o = V_{in}$ when $ABCD = 1$

Here V_o logic levels will be degraded by V_t effects.



$V_o = V_{in}$ when $A \oplus B \oplus C \oplus D \oplus E = 1$
CMOS 5-way Selector Switch:-

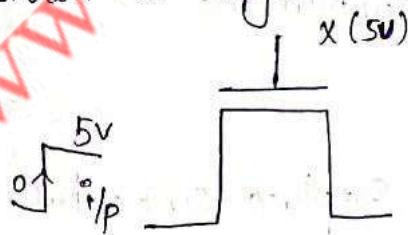


$$V_o = V_1 A + V_2 B + V_3 C + V_4 D + V_5 E$$

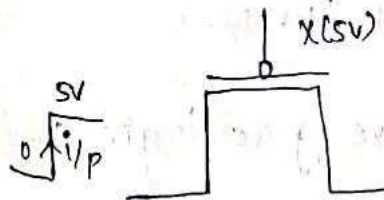
Assuming A, B, C, D, E are mutually exclusive i.e., V_{out} logic levels are not degraded by ' V_t ' effect.

Pass transistor and Transmission gates:-

Switches and switch logics may be formed from simple 'n' (or) p-type pass transistors in parallel as shown in figure below.



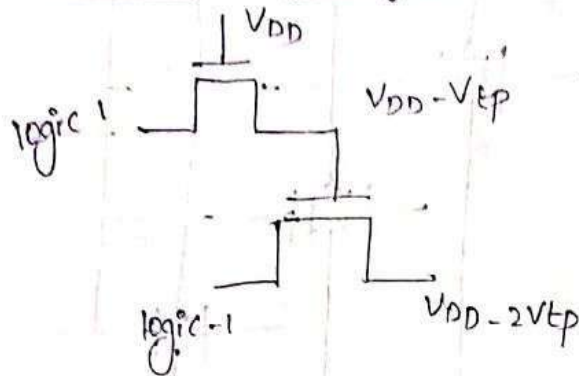
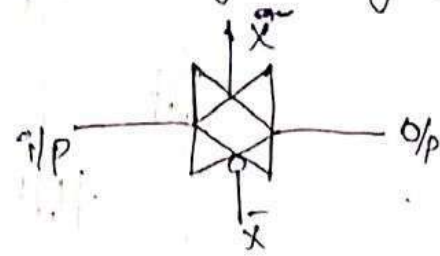
$V_{tp}(\downarrow) = 4V$ n-switch
 $\rightarrow \therefore$ degrades logic '1'



$V_{tp}(\uparrow) = 4V$ p-switch - degraded logic '0'



Transmission Gate Symbol:-



Loss of logic-1, if the gate of pass transistor is driven from another pass transistor.

fig:- Some properties of pass transistor and some logic families.

Alternative Gate Circuits (or) Gate Logic:-

CMOS Circuits suffer from increased area and corresponding increasing capacitance and delays logic gates becomes more complicate.

For this Reason, the designers develops the Circuits that can be used to Supplement the Complimentary Circuits.

There are not supposed to replace CMOS but can be used for some Special Purposes.

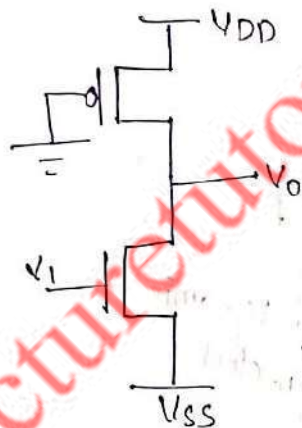
We have Several alternative gate logic circuits as listed below,

- (1) Pseudo nmos
- (2) Dynamic
- (3) C²mos (clocked cmos)
- (4) Domino logic
- (5) np cmos logic

pseudo nmos logic:-

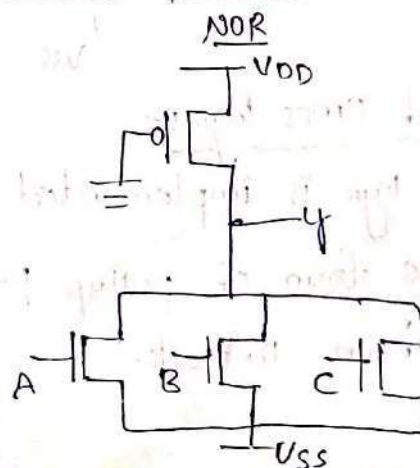
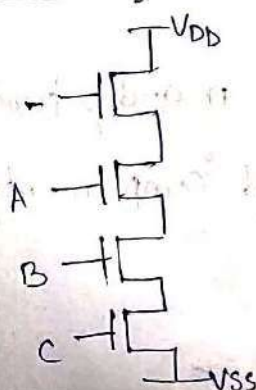
The pseudo nmos logic is one of the type of alternative gate circuits i.e., use to supplement for cmos circuits.

In this pseudo nmos circuit the depletion mode pull up mos transistor is replaced with p-mos transistor whose gate terminal is always ground.



Implementation of 3 Input NAND gate & NOR gates

Implementation of three i/p NOR gate and Nand gate using pseudo nmos logic:-



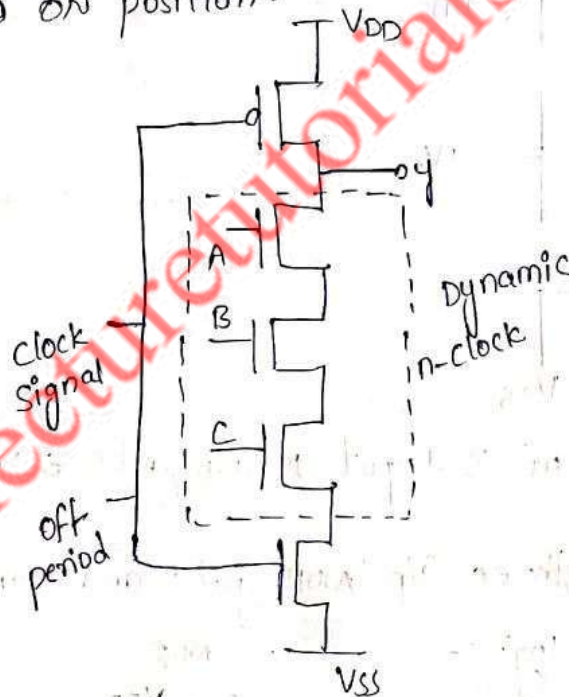
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Note: For 'n' numbers of inputs, Pseudo nmos logic requires 'n+1' numbers of transistors. Cmos logic require '2n' numbers of transistor.

Dynamic Cmos logic:-

The actual logic is implemented in the n-block and P transistor is used for non-time critical pre-charging output.

i.e. The output capacitance is charged to V_{DD} during off period of clock signal (ϕ).

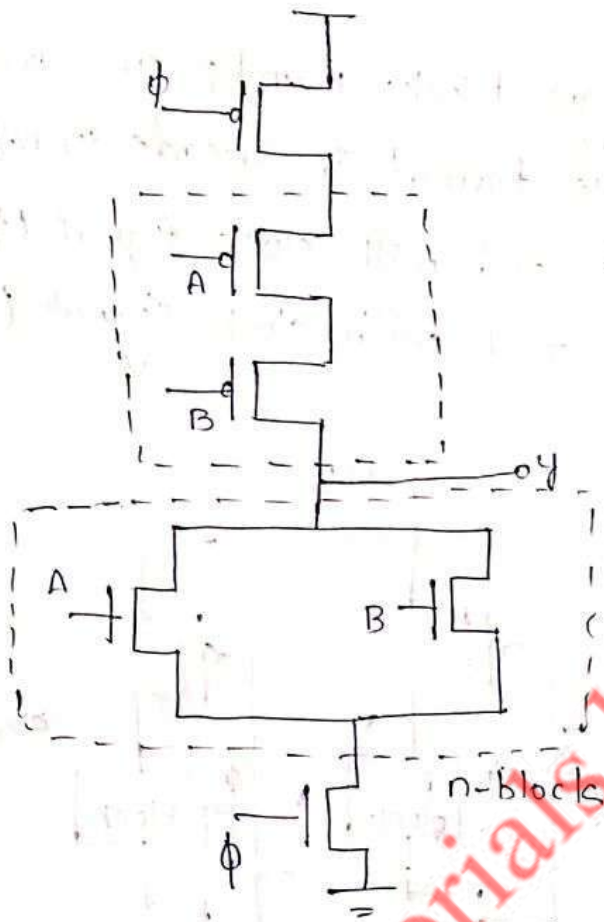
During this time, inputs due applied to n-block and state of logic is then evaluated during on period of clock when the bottom n-transistor is in on position.



Clocked Cmos logic:-

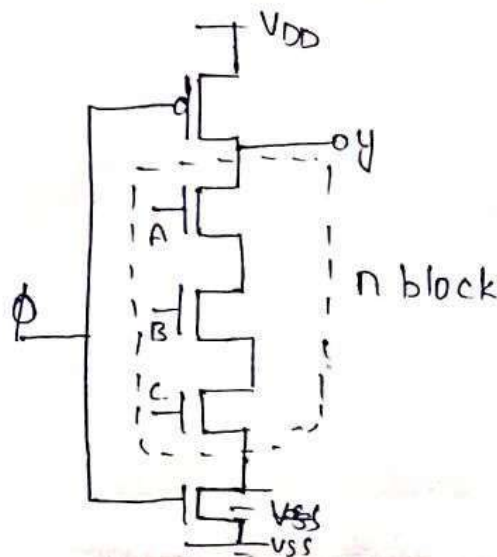
The logic is implemented in both n and p transistors in the form of pullup p-block and complimentary pull down n-block.

the logic in this circuit is evaluated only during the on period of clock.



Domino CMOS logic:-

An extension of dynamic CMOS logic is called domino CMOS logic. This is a modified arrangement that allows cascading of logic structures using only a single phase clock. So, at the output we use a buffer.



n_p cmos logic

This is another version of basic dynamic logic circuit.

The actual logic blocks n and p are arranged in the alternative format in cascade structure.

One block is fed with clock signal (ϕ) and another block is fed with clock signal ($\bar{\phi}$).

